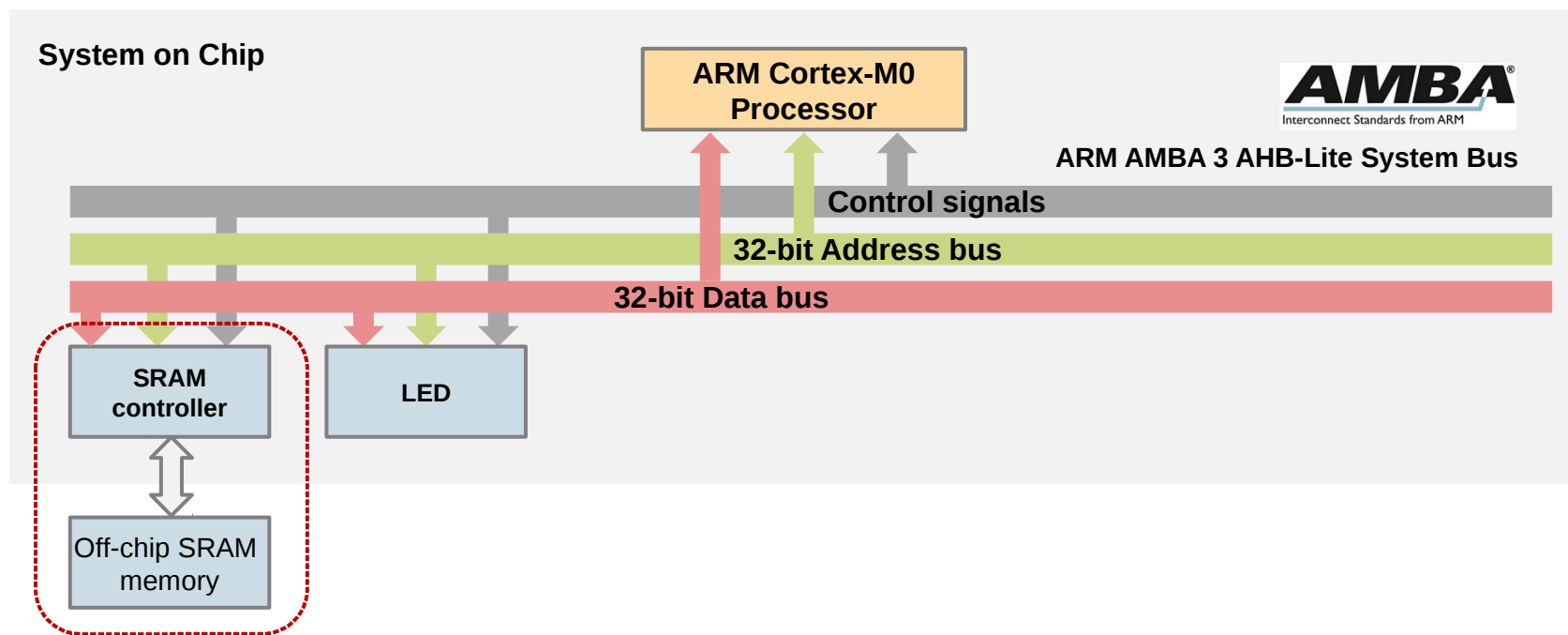


Design and Implementation of an AHB SRAM Memory Controller



Module Overview

- Learn the basics of Computer Memory;
- Design and implement an AHB SRAM memory controller, which replaces the previous on-chip memory;
- Memory controller testing using assembly;
- Lab Demonstration.



Module Syllabus

- Computer Memory
- Memory Types
- Volatile Vs. Non-volatile Memory
- Static RAM (SRAM)
- Dynamic RAM (DRAM)
- Non-volatile Memories
- Memory Controllers
- AHB SRAM Controller Hardware Implementation
- Lab Practice

Computer Memory

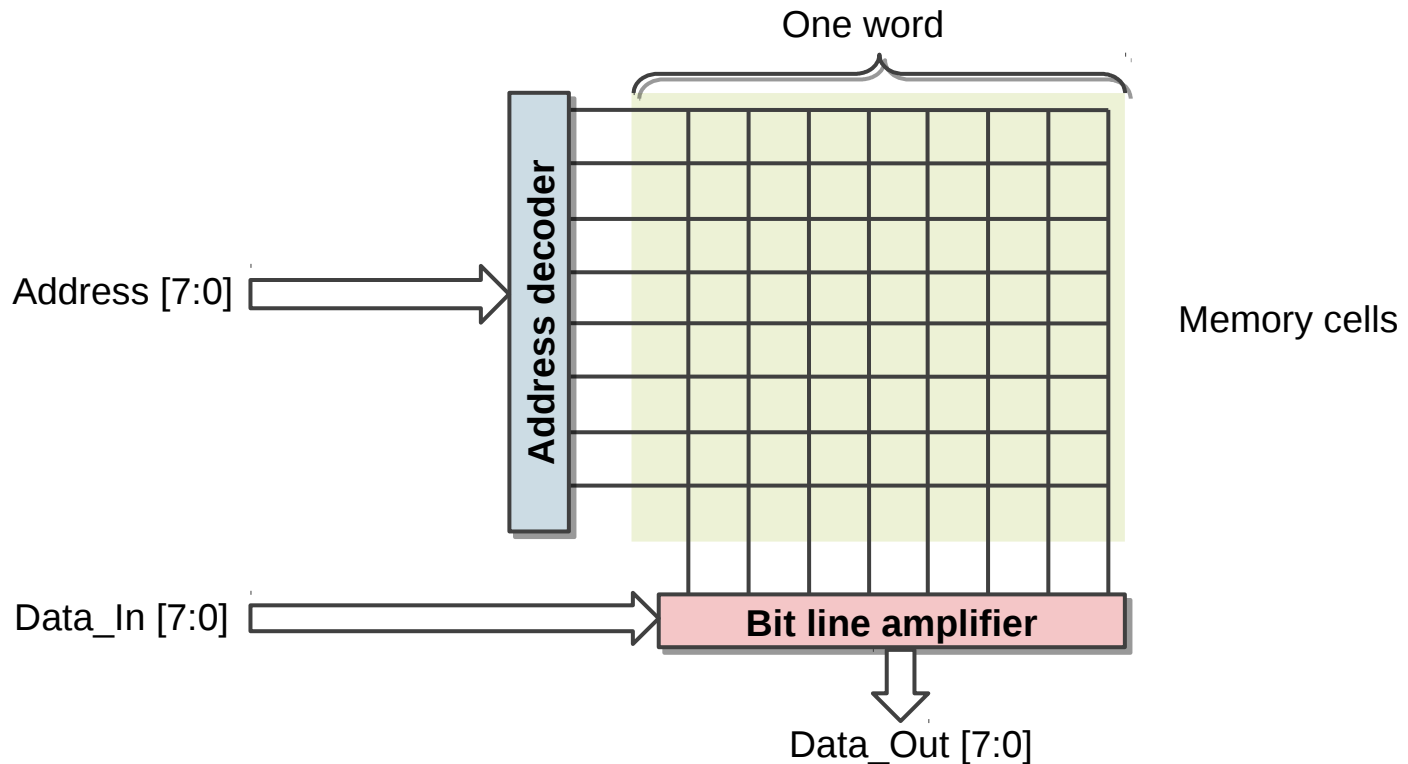
Computer Memory

- Computer Memory: a physical device that is used to store program code or data of a processor on either a temporary or a permanent basis
- Broadly, we can distinguish between two types of Memory
 - Volatile Memory
 - Requires power to keep the stored data;
 - Non-volatile Memory
 - Can retain stored data after power off



Computer Memory

- A memory is accessed by presenting it with an address, then writing or receiving the data at that address;
- For example, a memory architecture with 8-bit width and 8-bit data is shown below:



Memory Accessing

- Present an address:
 - Provide an address to the memory address bus;
 - A particular word is then selected by the address decoder and connected to the bit line amplifier;
 - For larger memory, the address may be divided into row and column sections;
- Read operation:
 - The selected data is connected to the bit line amplifier;
 - The amplifier restores the signal to the proper voltage level, then outputs it to the Data_Out port;
- Write operation:
 - Present the data to the Data_In port;
 - The amplifier set the bit lines to the desired values and drives that value from the bit line to the memory cell.

Volatile Vs. Non-volatile Memory

- Volatile memory

- Requires power to retain the data information;
- Usually faster access speed and less costly;
- Used for temporary data storage, such as CPU cache, internal memory;
- Also known as Random Access Memory (RAM);

- Non-volatile memory

- No power is required to retain the data information;
- Usually slower access speed and more costly;
- Used for secondary storage, or long-term persistent storage.

Types of Memory

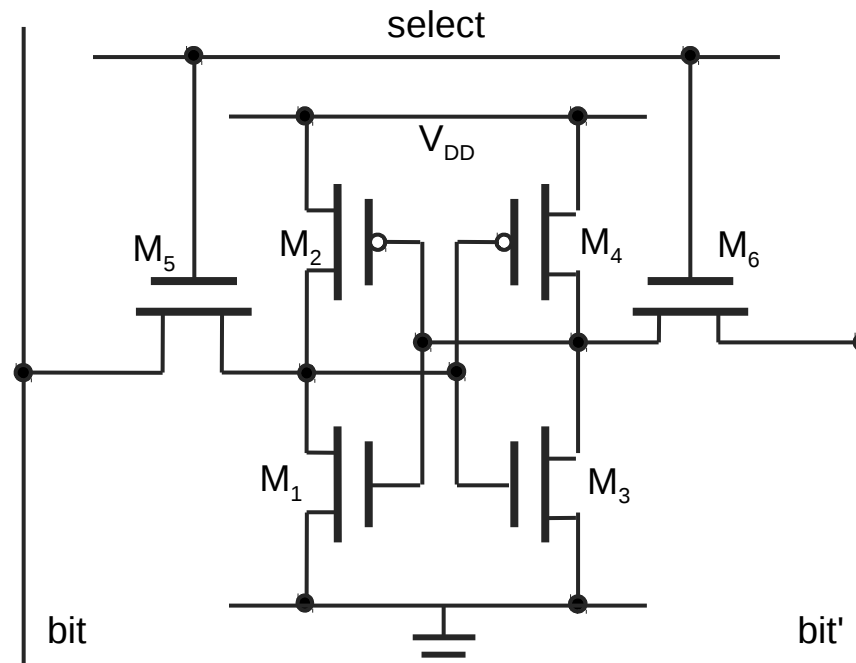
- Volatile memory
 - Static RAM (SRAM)
 - Dynamic RAM (DRAM)
- Non-volatile Memory
 - Read Only Memory (ROM)
 - Erasable Programmable ROM (EPROM)
 - Electrically Erasable Programmable ROM (EEPROM)
 - Non-volatile Random-access Memory (NVRAM)
 - Flash memory
 - Mechanical storage
 - Hard drive, magnetic tape

Static RAM

- Static RAM (SRAM)
 - Volatile memory
 - Data is retained as long as power is supplied;
 - Usually uses six transistors to store one bit data;
 - Fast data access;
 - Larger power consumption;
 - Less density, larger block size;
 - More expensive.

Static RAM

- An SRAM cell is typically made up of 6 MOSFET transistors;
 - A single bit is stored on 4 transistors (M1-M4), which form 2 inverters that are cross-coupled;
 - The access of the bit is controlled by two access transistors (M5 and M6), which are gated by the word line (select);



Accessing a Static RAM

- Read operation
 - The address is decoded and the desired cell is then selected, in which case the select line is set to one;
 - Depending on the value of the 4 transistors (M1-M4), one of the bit line will be charged to 1 and the other will be drained to 0;
 - The states of the two bit lines (bit and bit') are then read out as 1-bit data;
- Write operation
 - The two bit lines (bit and bit') are pre-charged to the desired value (e.g. bit = V_{DD} , bit' = V_{SS})
 - The address is decoded and the desired cell is then selected, in which case the select line is set to one;
 - The 4 transistors (M1-M4) are then forced to flip their states (either charged or discharged), since the bit lines normally have much higher capacitance than the 4 transistors;

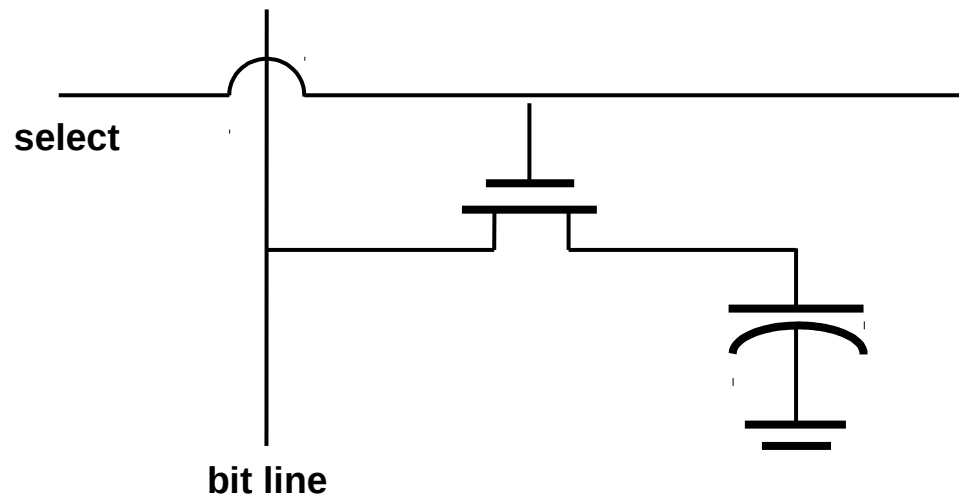
Dynamic RAM

- Dynamic RAM (DRAM)

- One bit of data can be stored in one transistor and capacitor pair, the status of the capacitor (charged or uncharged) indicates the bit state (1 or 0);
- Needs to be refreshed (or recharged) periodically since the capacitor leaks its charge, e.g. every 10 ms;
- Higher density, smaller block size;
- Less expensive;
- DRAM can be categorized according to its data rate and synchronization mode, for example:
 - Single Data Rate (SDR) and Double Data Rate (DDR);
 - Synchronous DRAM (SDRAM) and non-synchronous DRAM.

Dynamic RAM

- In DRAM, each memory cell requires less transistors, e.g. three-transistor cell or even one-transistor cell;
- For example, the one-transistor cell is composed by one transistor and one capacitor;
 - One-transistor – a gate transistor used to select a single cell;
 - One-capacitor – stores the value of a single bit.



Accessing a Dynamic RAM

■ Read operation

- The address decoder decodes the address and set the select line to one;
- The bit line is then changed according to the state of the capacitor. For example, if the capacitor is discharged, the current will flow from the bit line to the capacitor, whereby the voltage of the bit line will be lowered below the threshold;

■ Write operation

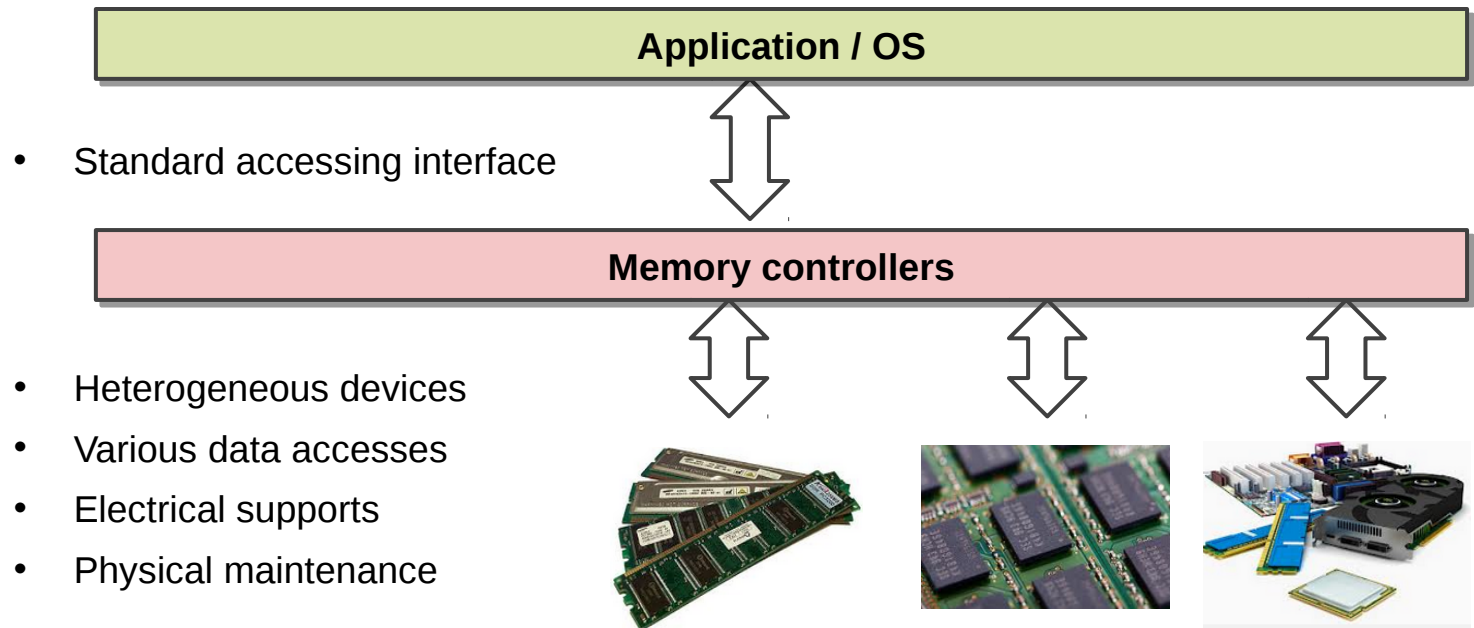
- The single bit line is pre-charged to a desired value (e.g. VDD or VSS);
- The address decoder decodes the address and set the select line to one;
- The capacitor is then either charged or discharged by the bit line;

Non-volatile Memory

- Read Only Memory (ROM)
 - In the early time, ROM is manufactured with desired data which cannot be changed;
 - Later types of ROM allow data to be reprogramed but with a degree of efforts, examples include
 - Erasable Programmable ROM (EPROM)
 - Electrically Erasable Programmable ROM (EEPROM)
- Non-volatile Random-access Memory (NVRAM)
 - Radom access, data can be both read and written;
 - Best-know form is flash memory.
- Mechanical storage
 - Non-electrically addressed memories, e,g, hard drive, magnetic tape, optical drive;
 - Less expensive but slower.

Memory Controller

- A memory controller is a piece of hardware that is mainly used for controlling the data flow going to/ from the memory block;
- Memory controllers facilitate the access to the heterogeneous physical devices, e.g. SRAM, DRAM, FLASH, hard disk etc...



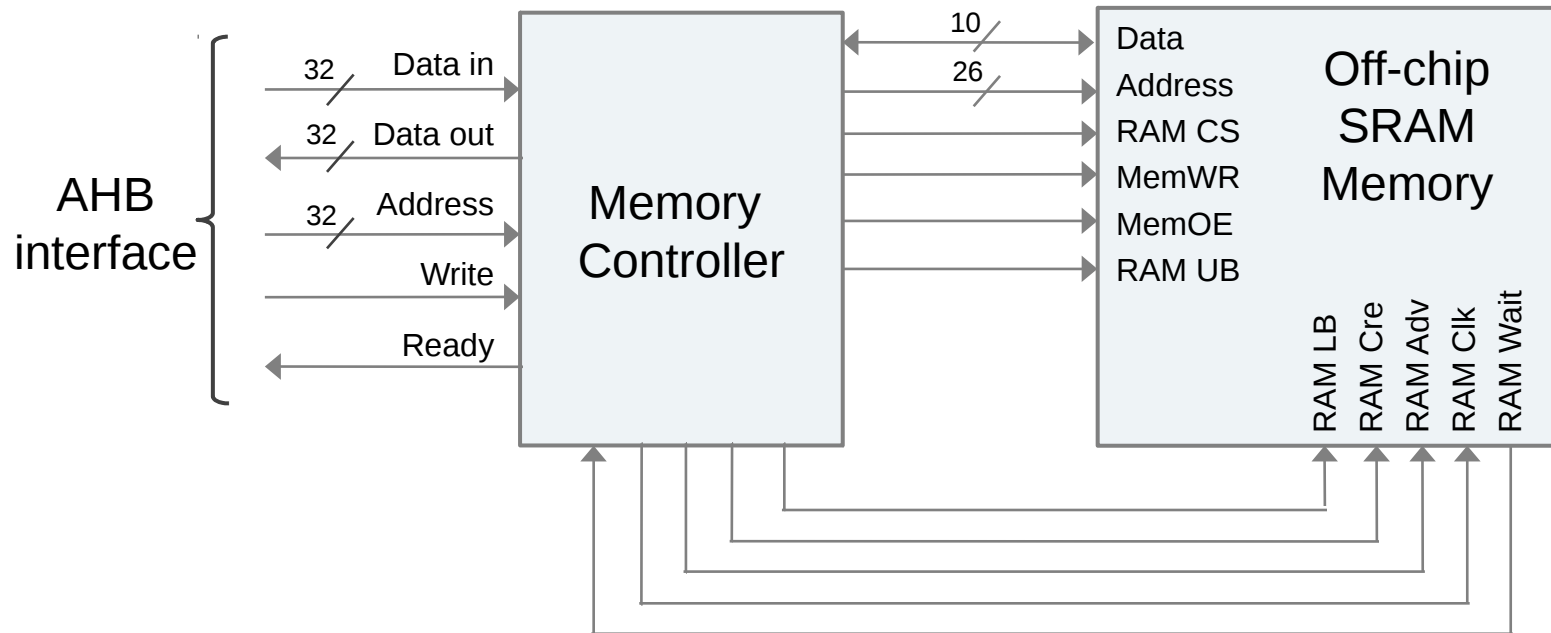
Memory Controller

- The role of a memory controller includes:
 - Interfacing with a particular type of memory block;
 - Facilitating the memory access by providing an universal interface to the system, e.g. to a standard bus interface;
 - Supporting a variety of memory access modes, such as burst mode, memory paging, etc...
 - May provide electrical supports for the memory, e.g. refreshing a DRAM.

AHB SRAM Controller Hardware Implementation

AHB SRAM Memory Controller

- In this set of teaching material, the off-chip memory on the target board is a 16MB cellular RAM from Micron, which has a SRAM-like interface with 16-bit bus width.

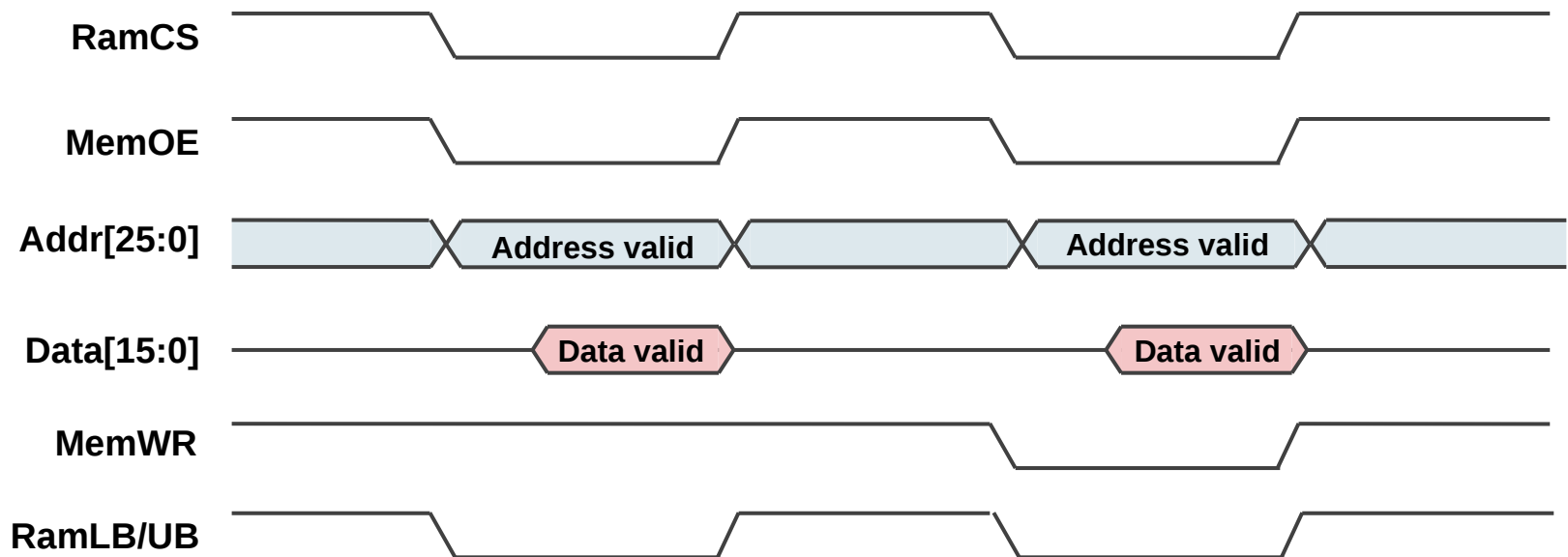


Signal Description

Name	IO	Description
Data[15:0]	IO	16-bit data input/ output bus
Addr[25:0]	I	26-bit address bus
RamCS	I	Chip select, activates the device when LOW
MemOE	I	Output enable: enable the output buffers when LOW
MemWR	I	Write enable: write to the memory when LOW
RamLB	I	Lower byte enable
RamUB	I	Upper byte enable
RamClk	I	Additional clock input used to synchronize with the system, can be set to LOW as it is not needed in this teaching material
RamAdv	I	Address valid: indicates that a valid address is given on to the address bus; can be set to LOW as it is not needed in this teaching material
RamCre	I	Control register enable, can be set to LOW as it is not needed in this teaching material
RamWait	O	Provides data-valid feedback in the burst mode, not needed in this teaching material

Example Timing

- The off-chip memory supports a variety of transfer mode, the following timing graph gives a basic read and write timing.
- The memory controller also has to cope with different data width, namely merging two 16-bit data from the memory to form a 32-bit data to be transferred through AHB bus.



Program the Device

- Once the memory controller is implemented, the off-chip SRAM can be used for the program memory; hence the program code can be updated without reconfiguring the FPGA chip.
- A variety of download utilities can be used to program the SRAM, such as Adept from Digilent and iMAPCT from Xilinx.

Lab Practice

Lab Practice

- Hardware design
 - Design and implement the peripheral (memory controller) in hardware using Verilog;
- Software programming
 - Test the peripheral using Cortex-M0 processor programmed in assembler language;
- System demonstrating
 - For example, toggle LEDs at a given frequency, using the SRAM controller.

Useful Resources

- Reference1

- Nexys3 Reference Manual:

http://www.digilentinc.com/Data/Products/NEXYS3/Nexys3_rm.pdf

- Reference2

- User Guide of Micron CellularRAM1.5 (MT45W8MW16BGX):

http://download.micron.com/pdf/datasheets/psram/16mb_asyncpage_cr1_0_p23z.pdf