

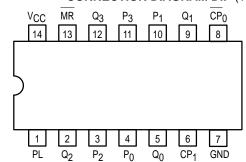
4-STAGE PRESETTABLE RIPPLE COUNTERS

The SN54/74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8, 4, 2, 1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54/74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset (MR) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (PL) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when PL is LOW and storing the data when PL is HIGH.

- Low Power Consumption Typically 80 mW
- High Counting Rates Typically 70 MHz
- Choice of Counting Modes BCD, Bi-Quinary, Binary
- Asynchronous Presettable
- Asynchronous Master Reset
- Easy Multistage Cascading
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOADING (Note a)

PIN NAMES

		HIGH	LOW
CP ₀	Clock (Active LOW Going Edge)	1.0 U.L.	1.5 U.L.
	Input to Divide-by-Two Section		
CP ₁ (LS196)	Clock (Active LOW Going Edge)	2.0 U.L.	1.75 U.L.
	Input to Divide-by-Five Section		
CP ₁ (LS197)	Clock (Active LOW Going Edge)	1.0 U.L.	0.8 U.L.
	Input to Divide-by-Eight Section		
MR	Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
PL	Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P ₀ -P ₃	Data Inputs	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Outputs (Notes b, c)	10 U.L.	5 (2.5) U.L.
NOTEO		!	3 1

a. 1 TTL Unit Load (U.L.) = 40µA HIGH/1.6 mA LOW.

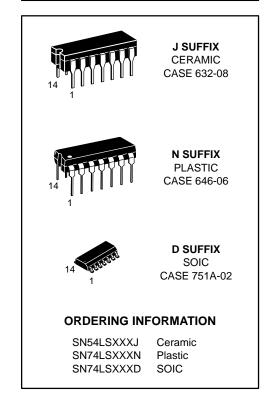
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74)
 Temperature Ranges.

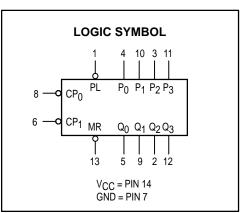
c. In addition to loading shown, Q₀ can also drive CP₁.

SN54/74LS196 SN54/74LS197

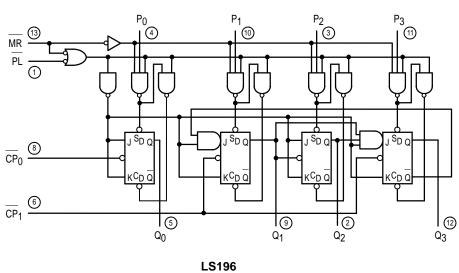
4-STAGE PRESETTABLE RIPPLE COUNTERS

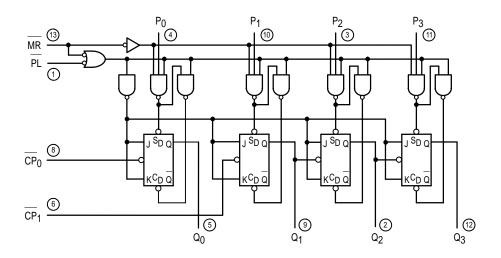
LOW POWER SCHOTTKY





LOGIC DIAGRAM





LS197

V_{CC} = PIN 14 GND = PIN 7 = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divideby-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The CPn input serves the Q₀ flip-flop in both circuit types while the CP₁ input serves the divide-by-five or divide-by-eight section. The Q₀ output is designed and specified to drive the rated fan-out plus the CP₁ input. With the input frequency connected to CP₀ and Q₀ driving CP₁, the LS197 forms a straightforward module-16 counter, with Q0 the least significant output and Q3 the most significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to CP_0 and with Q_0 driving CP_1 , the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to CP_1 and Q_3 driving CP_0 , Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (P_0-P_3) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the P_0 inputs will be reflected in the outputs.

DECADE (NOTE 1) BI-QUINARY (NOTE 2) COUNT Q_1 Qn COUNT Q_1 Q_3 Q2 Q_0 Q_3 Q_2 0 L L L L L L L L 1 L L L Н 1 L L L Н 2 L L Н L 2 L L Н L 3 3 Н L L Н Н L L Η Н Н 4 L L L 4 L L L 5 L Н L Н 5 Н L L L 6 L Η Н L 6 Н L L Н 7 7 L Н Н Н Н L Н L 8 8 Н Η Н L L L L Н 9 Н 9 Н Н Н L

Figure 2. LS196 COUNT SEQUENCES

NOTES:

MODE SELECT TABLE

	INPUTS	DESDONSE				
MR	PL	СР	RESPONSE			
L	Х	Х	Reset (Clear)			
Н	L	Х	Parallel Load			
Н	Н	l	Count			

H = HIGH Voltage Level

^{1.} Signal applied to CP₀, Q₀ connected to CP₁.

^{2.} Signal applied to CP₁, Q₃ connected to CP₀.

L = LOW Voltage Level

X = Don't Care

⁼ HIGH to Low Clock Transition

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				Limits					
Symbol	Parameter		Min	Тур	Max	Unit	Test Conditions		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
VIL	Input LOW Voltage 54				0.7	V		t LOW Voltage for	
*IL	Imput 2017 Voltago	74			0.8	Ů	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA		
V	Output HICH Voltage	54	2.5	3.5		V		= MAX, V _{IN} = V _{IH}	
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
V	Output I OW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$ $V_{IN} = V_{IL} \text{ or } V_{IH}$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	per Truth Table	
^I IH	Input HI <u>GH</u> Current <u>Data, PL</u> <u>MR, CP₀ (LS</u> 196) <u>MR, CP₀, CP₁ (LS197)</u> CP ₁ (LS196)				20 40 40 80	μА	$V_{CC} = MAX, V_{IN} = 2.7 V$		
	Data, PL MR, CP ₀ (LS196) MR, CP ₀ , CP ₁ (LS197) CP ₁ (LS196)				0.1 0.2 0.2 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V		
կլ	Input LO <u>W</u> Current Data, PL MR CP ₀ CP ₁ (LS196) CP ₁ (LS197)				-0.4 -0.8 -2.4 -2.8 -1.3	mA	V _{CC} = MAX, V _{IN}	J = 0.4 V	
los	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX		
Icc	Power Supply Current				27	mA	$V_{CC} = MAX$		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

				Lin						
			LS196			LS197				
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Unit	Test Conditions	
f _{MAX}	Maximum Clock Frequency	30	40		30	40		MHz		
^t PLH ^t PHL	CP ₀ Input to Q ₀ Output		8.0 13	15 20		8.0 14	15 21	ns		
^t PLH ^t PHL	CP ₁ Input to Q ₁ Output		16 22	24 33		12 23	19 35	ns		
^t PLH ^t PHL	CP ₁ Input to Q ₂ Output		38 41	57 62		34 42	51 63	ns	V _{CC} = 5.0 V	
^t PLH ^t PHL	CP ₁ Input to Q ₃ Output		12 30	18 45		55 63	78 95	ns	V _{CC} = 5.0 V C _L = 15 pF	
^t PLH ^t PHL	Data to Output		20 29	30 44		18 29	27 44	ns		
^t PLH ^t PHL	PL Input to Any Output		27 30	41 45		26 30	39 45	ns]	
^t PHL	MR Input to Any Output		34	51		34	51	ns		

AC SETUP REQUIREMENTS $(T_A = 25^{\circ}C)$

		Limits							
		LS196		LS197					
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Unit	Test Conditions
t _W	CP ₀ Pulse Width	20			20			ns	
t _W	CP ₁ Pulse Width	30			30			ns	
t _W	PL Pulse Width	20			20			ns	
t _W	MR Pulse Width	15			15			ns	
t _S	Data Input Setup Time — HIGH	10			10			ns	V _{CC} = 5.0 V
t _S	Data Input Setup Time — LOW	15			15			ns	
^t h	Data Hold Time — HIGH	10			10			ns	
t _h	Data Hold Time — LOW	10			10			ns	
t _{rec}	Recovery Time	30			30			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recog-

nition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

RECOVERY TIME (t_{FeC}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

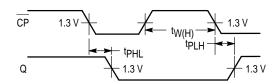
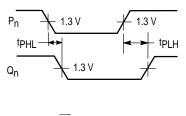


Figure 1



NOTE: PL = LOW

Figure 2

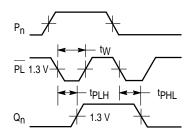


Figure 3

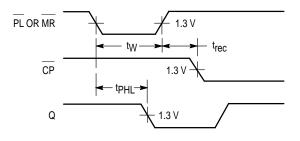
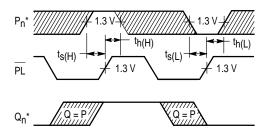


Figure 4



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 5