Boolean Board

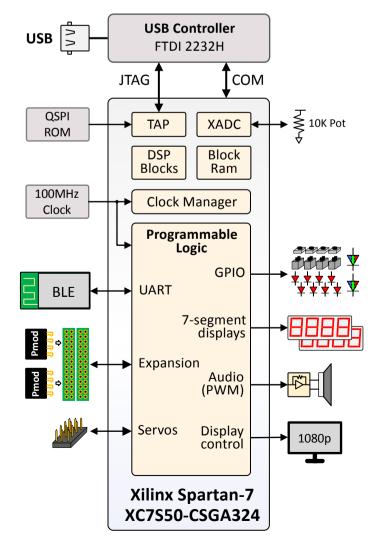
Complete Reference Manual



The Boolean board is a configurable digital logic system designed specifically for teaching and learning digital logic design. The board is centered on a Xilinx Spartan-7 FPGA (XC7S50) that can be configured into a virtually unlimited number of hardware circuits. The Spartan-7 FPGA includes:

- more than 8,000 FPGA slices, each containing four 6-input look-up tables and 8 flip-flops, equivalent to 52K logic cells;
- 120 DSP blocks, each with dual 24-bit adders, a 2's compliment multiplier, and a 48-bit accumulator;
- 337Kbytes of high-speed, dual port RAM;
- Five clock management tiles that can generate a wide variety of clock signals from a single outside source;
- A 12-bit, 1MSPS analog-to-digital converter;
- And many other circuits and functions.

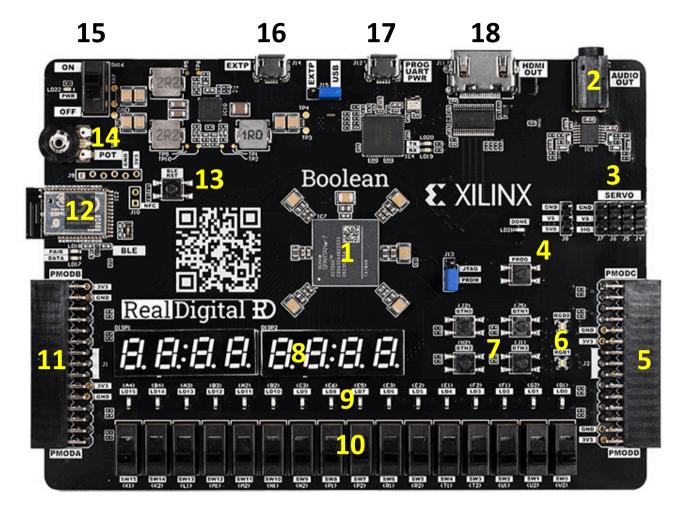
The Boolean board surrounds the FPGA chip with several peripheral devices, including push buttons, slide switches, discrete and RGB LEDs, an 8-digit seven-segment display, audio and video outputs and an optional Bluetooth radio – everything needed to implement a wide variety of digital circuits and systems without the need for any other components. Two 30-pin expansion connectors, both capable of driving two Pmods as well as custom peripheral boards, provide easy access to an additional 44 FPGA I/O pins.



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Figure 1. Boolean board diagram

Xilinx's Vivado Webpack software provides a full-featured environment for circuit design, simulation, and implementation. Vivado supports both Verilog and VHDL, and includes an HDL editing and debug environment, a simulator, a synthesizer, an FPGA programming interface and hardware debugging tool (a logic analyzer). The Boolean board can be directly programmed from within Vivado, and the tools are freely downloadable from the Xilinx website.



1	Spartan-7 XC7S50-CSGA324 FPGA	10	16 slide switches
2	Audio output	11	Expansion connector (30-pin)
3	Servo motor connectors (x4)	12	BLE radio module
4	FPGA Program button (reset)	13	BLE reset button
5	Expansion connector (30-pin)	14	10K Potentiometer (connected to ADC)
6	2 RGB LEDs	15	Power switch
7	4 pushbuttons	16	Accessory power connector
8	8-digit seven-segment display	17	Main USB (power, programming, UART)
9	16 discrete LEDs	18	HDMI source (up to 1080P)

Figure 2. Boolean board high-level view

When the Boolean board is first powered on, the FPGA must be configured before the board can do anything. In a typical interactive design environment like a classroom setting, the FPGA is programmed from Vivado. The FPGA can also be configured automatically from an on-board ROM at power-on if jumper block J13 is set to "PROM" (see below). The ROM can also be programmed from Vivado. The Boolean board ships with an example design programmed into the ROM, so board function can be verified right out of the box.

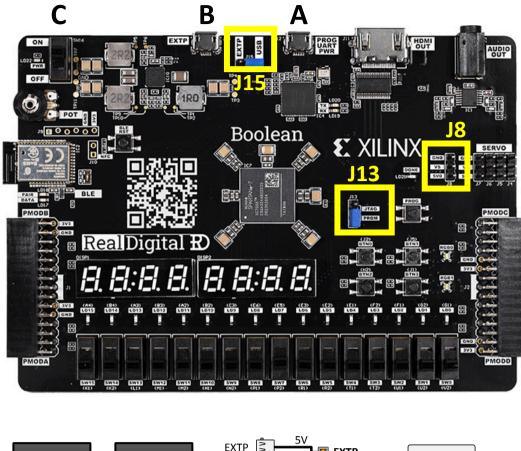
Setting up the Boolean Board

To set up the Boolean board for use, a programming cable must be attached and power must be applied. Typically, a single USB cable attached to the "PROG UART" USB connector (labeled A in the picture below) provides power and a programming port. A jumper block between the two USB connectors selects which connector supplies board power.

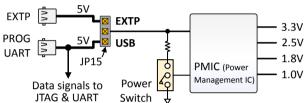
Note: A "jumper" is a small, removable connector that creates a connection between adjacent pins on a header/connector - it performs the same function as a switch, but it's smaller, cheaper, and less likely to be accidently moved from one position to another.

Jumpers

Most typically, **J15** is set to USB so that the board draws power from same USB cable that is used for programming. If **J13** is set to PROM, the FPGA will be automatically configured from the on-board ROM at power-on. Regardless of J13's setting, the board can always be programmed from Vivado (via JTAG) by connecting a micro-USB cable to the PROG/UART port. J8 selects the power source for any connected servo motors. If no servo motors are used, then no jumper is needed on J8. When servo motors are being used, it is typical to use an external power supply, and so J8 would be set to EXTP.











Boot from JTAG/PC Boot from ROM J13 Settings (Programming Mode)

Boolean Board Power Delivery Schematic



Figure 3. Boolean board jumper blocks and Power Delivery

JTAG & UART

Power

Power is applied using one of two micro-USB connectors. The primary connector A (labeled PROG UART in the silkscreen) provides power as well as a USB port for JTAG programming and UART communications. In most cases, this is the only connection needed.

If more power is needed (for example, to drive a servo motor or plug-in peripheral boards), a plug-in power supply capable of proving more current can be connected to the EXTP USB port (B in the figure). Only power is drawn from this connector (the data signals are not connected), so any USB charger plug can be used. Whichever USB connector is used, the power switch labeled C will turn the board on or off.

To draw power from the primary USB port, set jumper J15 to USB; to use external power set it to EXTP. Overall power consumption is dependent on the board's configuration. Most designs, and especially the Real Digital design projects, will draw less than 300mA.

Programming

During programming, a ".bit" file is transferred to the FPGA to configure its internal programmable elements. Bit files are produced when Vivado synthesizes and implements Verilog or VHDL source files. They can be transferred directly from Vivado to the FPGA via the USB port, or programmed into the on-board ROM so the FPGA can be automatically configured at the next power/reset cycle. Detailed guidelines for producing a Vivado project and source files, and for programming the Boolean board are available here: A First Vivado Project For The Boolean Board

Jumper J13 selects the programming source. Placing J13 on the "JTAG" setting will disable ROM programming, and the FPGA will remain idle until configured from Vivado. Placing J13 on the "PROM" setting will cause the FPGA to automatically load from ROM at power-on. After the FPGA is programmed from ROM, it can still be reprogrammed from Vivado via USB.

GPIO

The term "General Purpose Input/Output" (GPIO) generally refers to digital input signals driven by two-state devices like slide switches or pushbuttons, or output signals that drive an indicator device (like an LED). The Boolean board includes 16 single-pole double-throw (SPDT) slide switches, 4 momentary single-pole single-throw (SPST) pushbutton switches, 16 single-color LEDs, and 2 tri-color (RGB) LEDs.

The slide switches output a constant '0' or a '1' depending on their position. The pushbuttons are normally open, and so normally output a '0' when not pressed, and output a '1' only while actively pressed. All switches are connected to FPGA pins through series resistors to prevent damage from inadvertent short circuits.

All LED signals are active high. The individual/discrete LEDs are connected to FPGA pins via 330-ohm resistors, so a logic high signal (3.3V) will illuminate them with about 1mA of current. RGB LEDs have higher voltage thresholds and different current requirements, and so they are driven by transistors. A logic high on any RGB LED signal drives the transistor base and causes about 5mA of current to flow through the LED.

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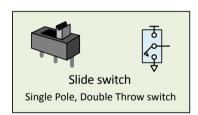
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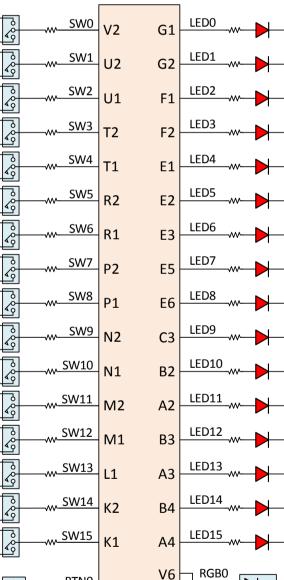
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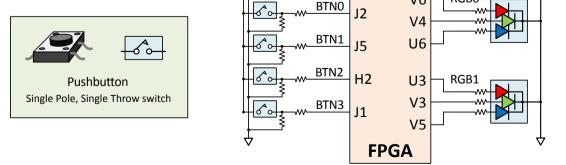


Figure 4. Boolean GPIO devices

Each RGB LED device includes three individual LEDs that are located very close together, giving the appearance of a single LED. Each LED is driven independently, and this allows different colors to be created. By simply turning LEDs on or off, seven different colors can be created. But by controlling the brightness levels of individual LEDs, a broad range of colors can be created. LED brightness levels are typically controlled using pulse-width modulated (PWM)

signals. PWM signals are commonly used as simple "digital to analog" converters - when used to control LED brightness, the PWM signals turn individual LEDs on and off at a frequency higher than the human eye can detect, with different lengths of "on" time to create the appearance of different brightness levels. Users can define custom

PWM IP blocks to drive the LEDs - you can read more about PWM circuits here: PWM And PDM Signals

Seven Segment Display

A seven-segment display is built from individual LED's arranged in a figure-8 pattern as shown. Any LED/segment can be individually illuminated, so any one of 128 different patterns can be shown. The figure below shows segment illumination patterns for decimal and hexadecimal digits.

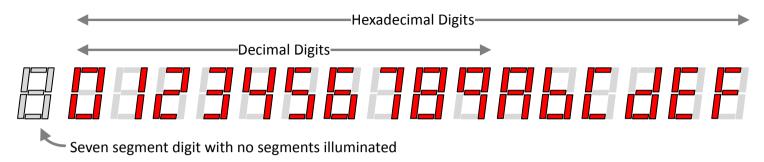


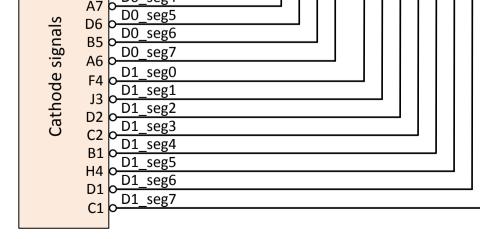
Figure 5. Seven segment display illuminatation patterns

The Boolean board includes two 4-digit seven-segment displays (8 total digits) that use a common anode configuration. Segment LEDs consume about 3mA each (well within the current sourcing capability of the FPGA pins), so the cathodes are tied directly to FPGA pins. Since 24mA+ can flow through the anode signals, the anodes are driven from transistors that can provide the needed current (and the transistors are driven from the FPGA pins). All signals are active low.

To drive a single digit, the corresponding anode signal can be driven (low), and then individual cathodes can be driven (also low) to turn on individual segments. To drive all digits to create an eight-digit display, a scanning display controller is needed. To learn more about seven segment displays, including an example design of a seven-segment

controller, see the "Seven segment controller" document: Seven Segment Display

Vdd D1_a0 H3 D1 a1 J4 Anode signals D1 a2 F3 D1_a3 E4 Vdd Anodes D0_a0 D5 D0_a1 C4 D0 a2 C7 D0 a3 **SO** A8 **S5 FPGA S6** D0_seg0 **S4** D7 D0_seg1 C5 D0 seg2 A5 D0_seg3 Β7 D0_seg4



Cathode signals

Figure 6. Seven segment display

Clock

The Boolean board includes a 100MHz 50PPM MEMS/CMOS oscillator that is always running. The oscillator is connected to a multi-region clock-capable (MRCC) FPGA I/O pin (pin F14). From that pin, the clock signal can route to a clock management tile and/or to any flip-flop in the FPGA using the internal high-speed clock network.

Expansion Connectors

Two 100-mil-spaced dual rows of 30 through-holes are available to bring FPGA signals to expansion boards. Of the 30 holes, 4 are connected to ground, 4 to Vdd, and 22 to FPGA signals. All 22 FPGA signals are routed as differential pairs. The connector signals are organized so that two 12-pin Pmod connectors can be inserted into the marked subsets of holes, or one larger 30-pin connector can be used.

The holes are slightly offset so that though-hole connectors can be inserted and make adequate contact without the need for solder. If the connectors will be used long-term, or if there will be multiple insertion/removal cycles, or if a more reliable connection is required, the connectors should be soldered in place.

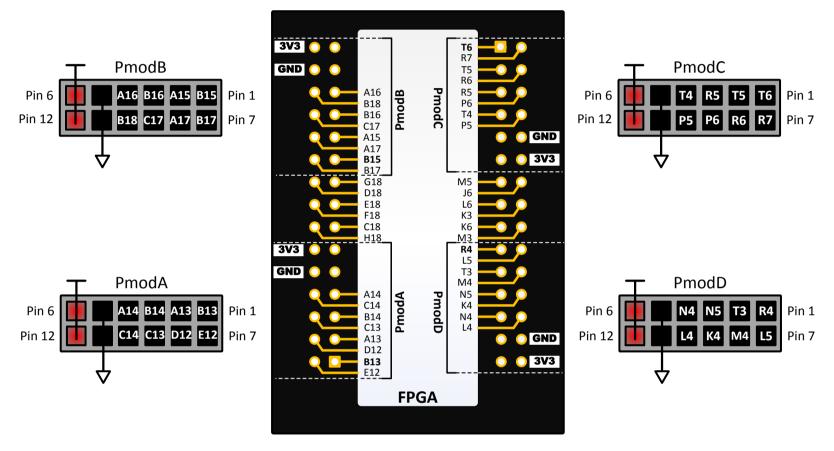


Figure 7. Boolean board expansion connectors

Audio port

The Boolean board includes two identical audio amplifier/filter circuits that drive the left and right channels of a 1/8" (3.5mm) stereo audio jack. The AC-couped amplifier channels include a 50Hz-5KHz bandpass filter designed to accommodate simple square waves or PWM/PDM encoded audio signals. For more on PWM/PDM signals:

PWM And PDM Signals

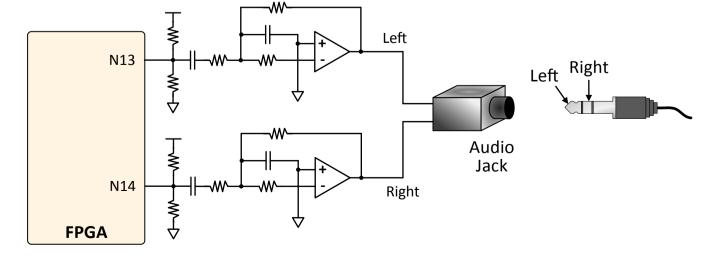


Figure 8. Boolean board audio output circuits

Bluetooth Radio

The Boolean board includes a Bluetooth 5.0 Low Energy (BLE) radio module based on the advanced Nordic Semiconductor nRF52832 device. The BLE module exchanges data with the FPGA using a simple two-wire UART/serial protocol (RXD/TXD) running at 115,200 bps. Send and Receive data packets can be up to 256 bytes, and are terminated with a newline (\n) character. Data sent from the FPGA is held in a FIFO within the BLE module, and transmitted immediately after a newline is encountered.

The PAIR LED will blink when the BLE radio is ready to be paired to your phone or host computer. Once it is paired, the PAIR LED will be on constantly. If the radio is not paired within one minute, it will enter a deep sleep mode. To wake up the module, press the **BLE RST** located beside the BLE module.

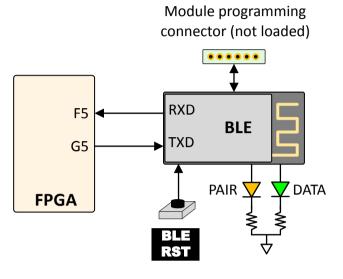


Figure 9. Boolean board BLE radio

HDMI port

Analog/VGA displays are becoming rare, so the Boolean board includes an HDMI source connector to support video controller design projects. Because HDMI display controllers are more complex than analog/VGA controllers, Real Digital provides a VGA-to-HDMI IP block. Using this IP block, users can design a typical VGA controller with resolutions up to 1280x720, and use it to drive the HDMI connector via the VGA-to-HDMI IP block.

The VGA-to-HDMI core receives the VGA timing signals HSync, VSync, and VDE (Video Display Enable), and video data signals (R, G, and B) with up to 8 bits per color. These signals are mapped into HDMI timing and data signals, effectively allowing HDMI controller details to be ignored. Details on accessing and using the VGA-to-HDMI IP block are available in the link. An additional link provides background information on creating a VGA controller circuit.

VGA To HDMI Analog And Digital Displays Clocking Wizard

In addition to the VGA timing and data signals, one additional clock signal running at 5X the pixel clock is needed. This faster clock can be produced using one of the Clock Management Tile IP blocks available in FPGA. Details on configuring and instantiating the CMT IP block are available in the link.

To ensure the video controller can reliably drive displays of at least 720p, a TI HDMI transmitter is used between the FPGA and the HDMI connector.

The figure below shows a block diagram of a display controller based on a VGA controller driving the VGA-to-HDMI IP block. In the FPGA block shown in the figure, the VGA Controller is user-designed IP, and the CMT and VGA to HDMI blocks are pre-existing IP blocks that only need to be configured and instantiated. All three blocks can then be assembled in a higher-level HDL module as shown in the example code.

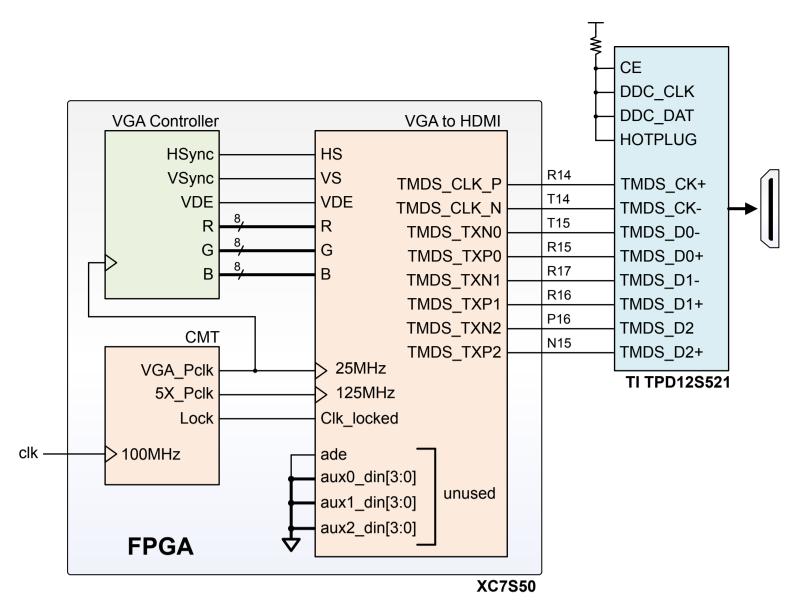


Figure 10. HDMI controller top-level block diagram

Servomotor Connectors

The Boolean board includes four 3-pin connectors that are compatible with standard hobby servo motors. Servo motors can draw up to several hundred milliamps each. Depending on the power available from the USB connector, the Boolean board's main power supply may be able to drive one or two servo motors (note the main power supply may come from the USB cable used to program the board, or from a separate, external USB wall-plug). Servo power routes through jumper J8. To use the main power supply, load a jumper at J8 across the VS/5V pin headers. If more power is needed, a two-pin MTE cable can connect a bench supply to J8 pins VS and GND as shown.

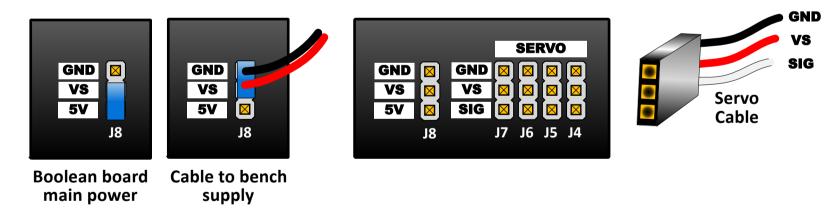


Figure 11. Boolean board servomotor connections

Servomotors are controlled with a single PWM signal that obeys a well-defined protocol (the signal is labeled SIG on

the Boolean board's servo connectors). You can learn more about servo motors and their control here:

Servomotors

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