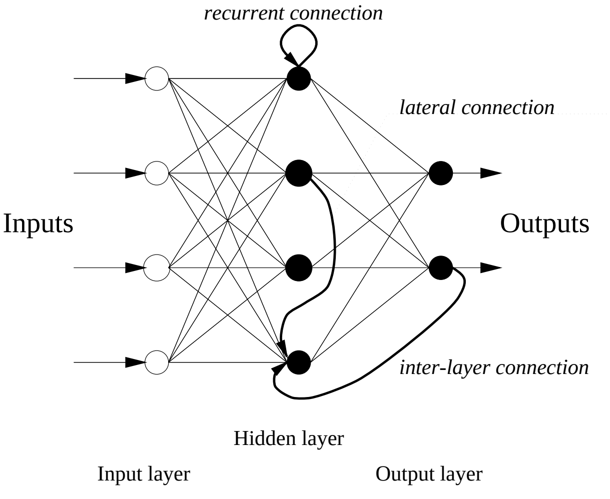
Nonlinear Digital Signal Processing
Neural Networks

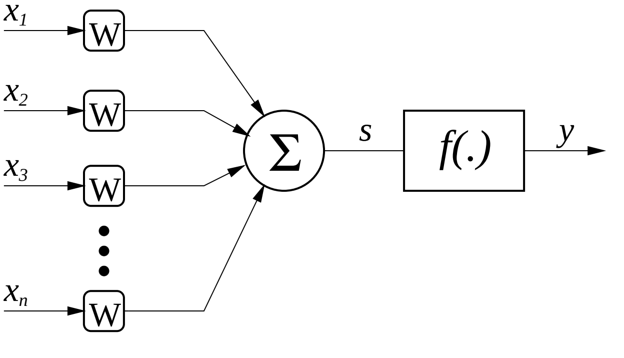
TUB-DMIS

Overview of Neural Networks

General neural network topology



General Structure of a Neuron



Operation modes:

- learning phase
- recall phase

Taxonomy of Neural Network Families

By training method

- *Supervised learning networks*
- *Unsupervised learning networks*
- *Fixed network*

By topology

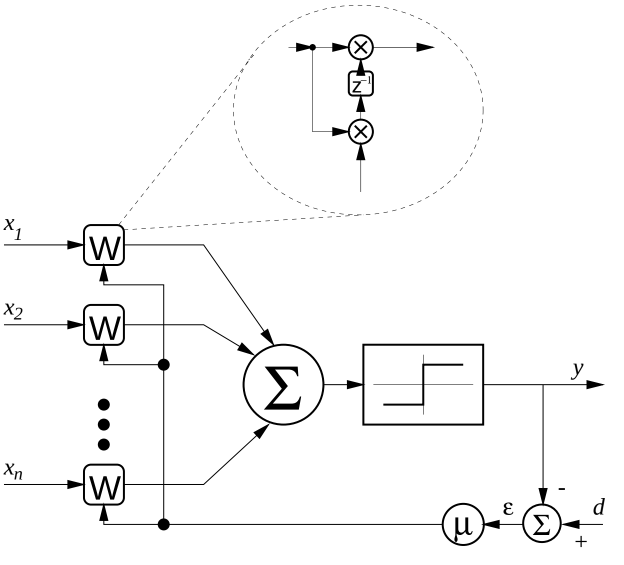
- *Feedforward networks*
- *Feedback networks*

By dynamics

- *Static networks*
- *Dynamic networks*
- *Temporal networks*

Some Important Network Types

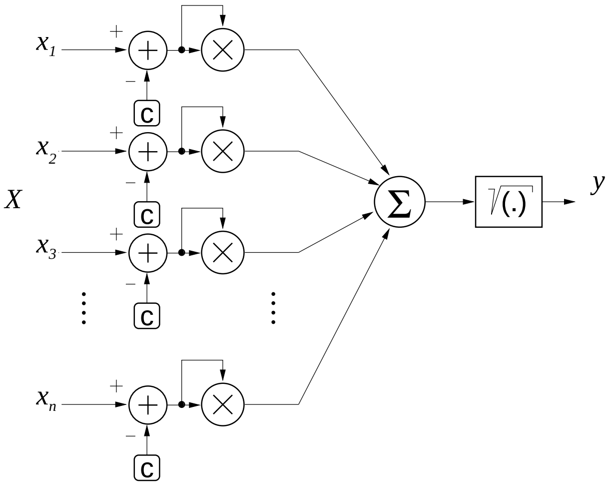
Perceptron



Adaline

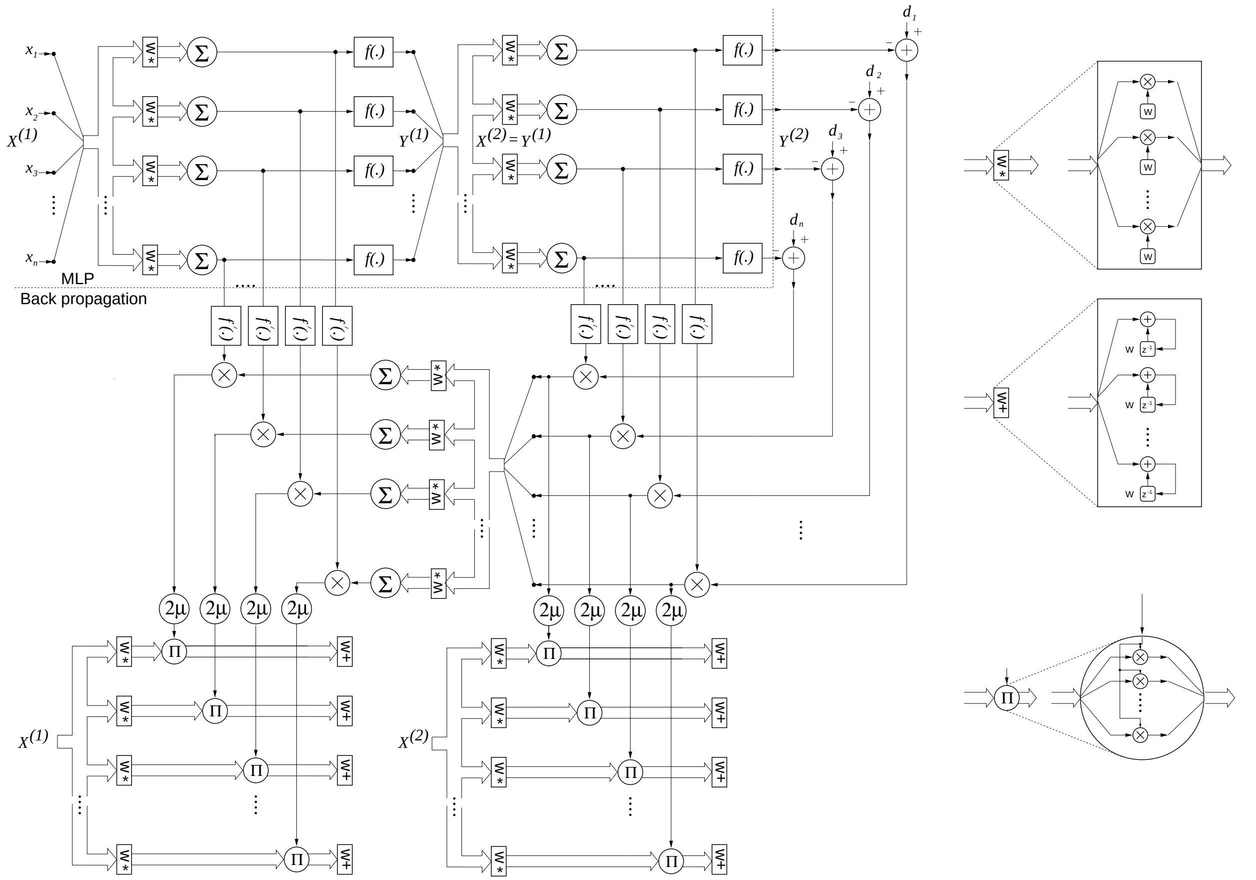
Kohonen Self-Organizing Map

Radial Basis Function network, RBF



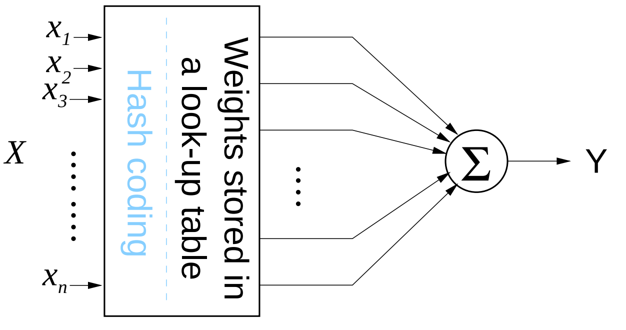
Some Important Network Types

Multi Layer Perceptron with Back-Propagation, MLP-BP

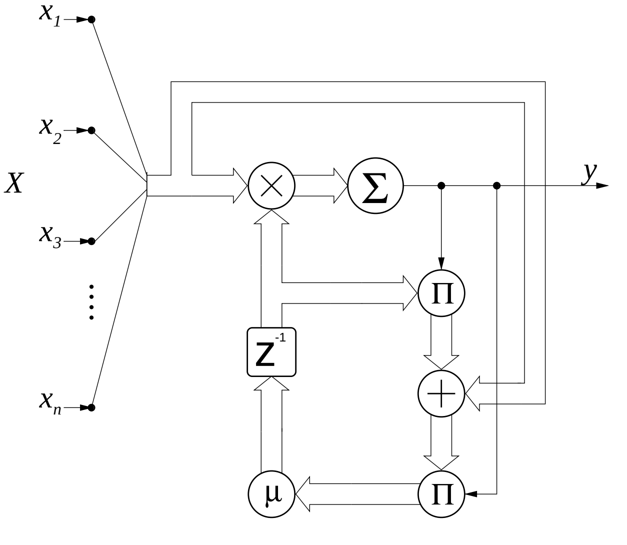

MLP
Back propagation

Some Important Network Types

CMAC network

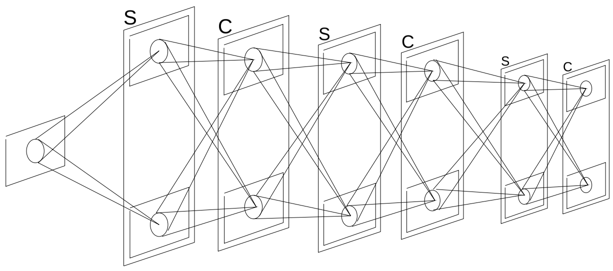


Principal Component Analysis networks, PCA

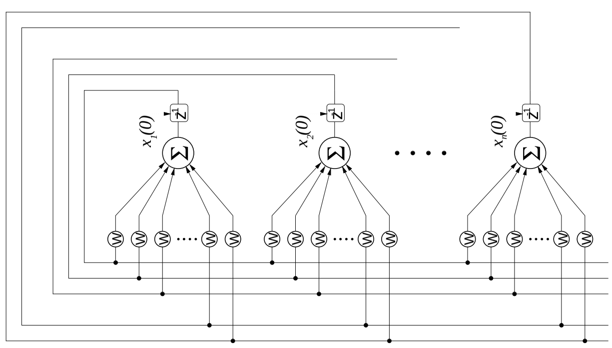


Some Important Network Types

Neocognitron



Hopfield network

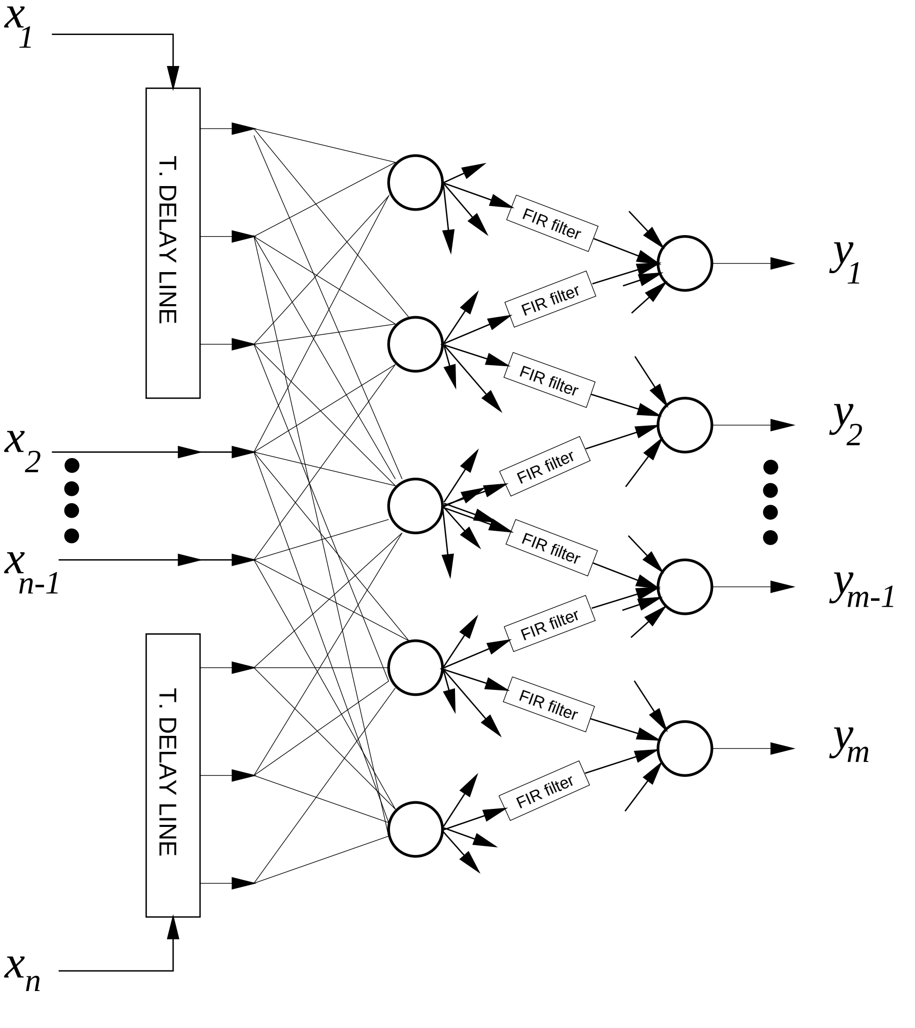


Boltzmann machine

Cellular Neural Network, CNN

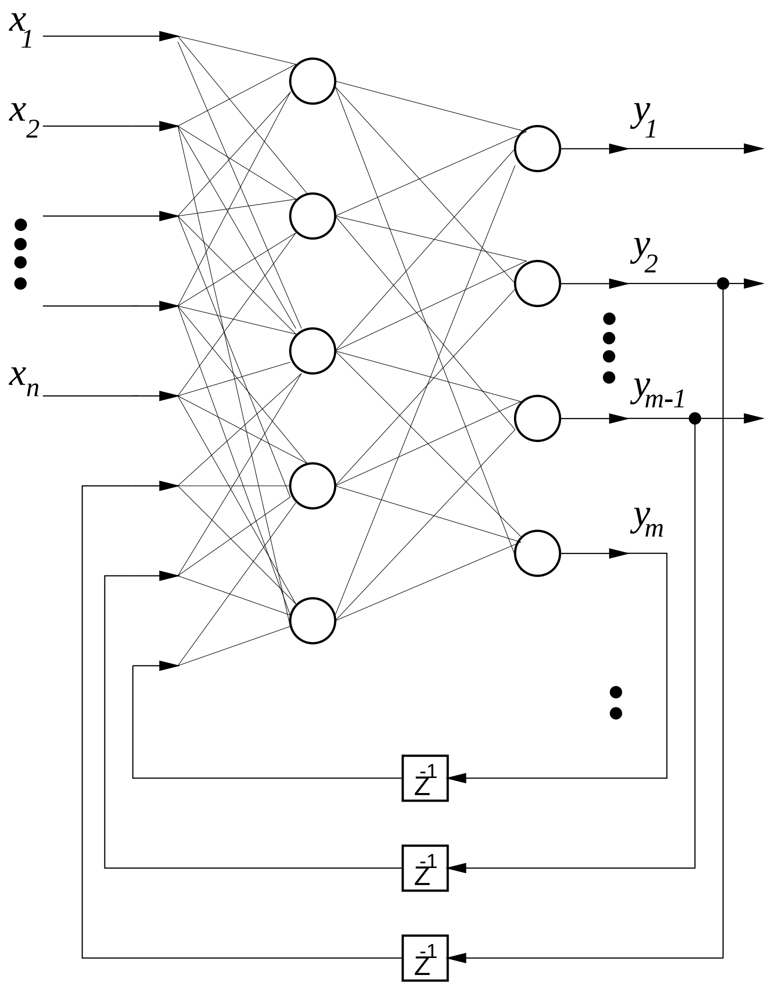
Some Important Network Types

Time-Delay Neural Network, TDNN



Some Important Network Types

Recurrent Neural Network RNN



Implementation Issues of Neural Networks

Taxonomy of implementations

Application point of view

- **Simulators**
  - Template simulators
  - Non-template simulators
  - Network specific simulators
- **"Real-world" applications**

By measure of parallelism

- **Sequential implementations**
- **Parallel implementations**

By tools

- **Software tools**
- **Hardware tools**

Parallelism in Neuro-implementations

- *Network parallelism*
  - layer parallelism
  - node parallelism
  - weight parallelism

- *Training parallelism*

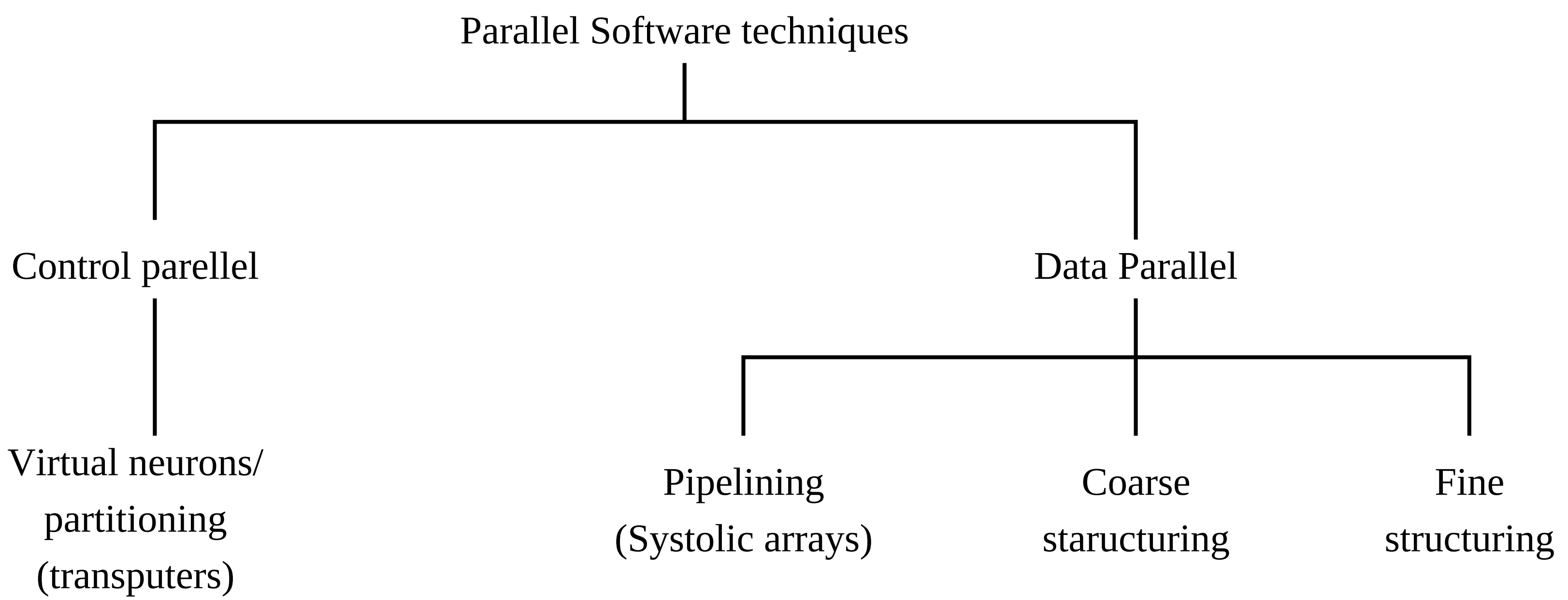
Parallelism in software implementations

- Compile-time decomposition
- Regular decomposition
- Possibility of purely local data flow
- Reuse of data

Parallelism in hardware implementations

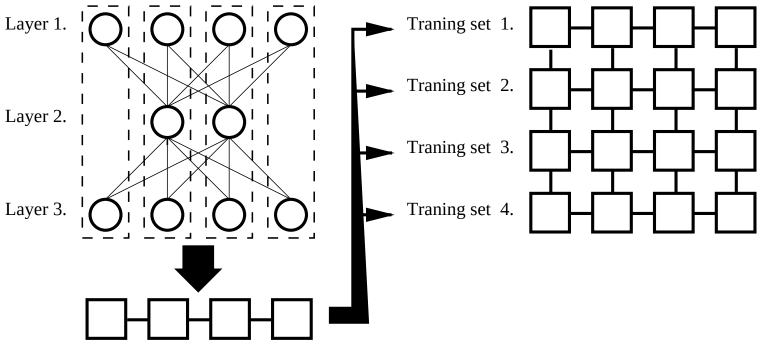
- Weight Parallel or Weight Serial
- Neuron Parallel or Neuron Serial
- Layer Parallel of Layer Serial
- SubNetwork Serial

Parallel Software Techniques

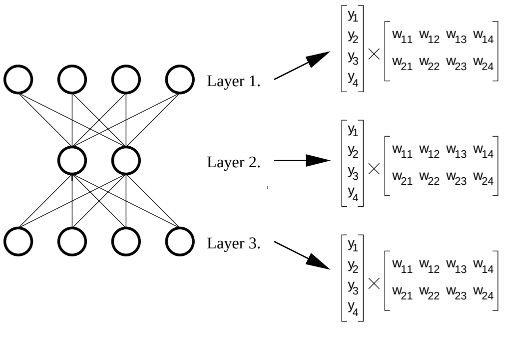


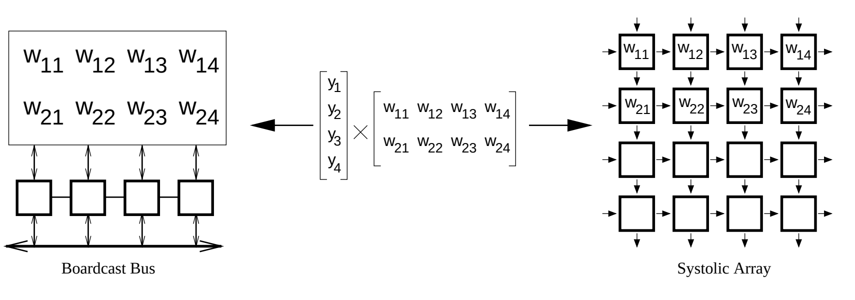
Parallel Software Techniques

Coarse structuring



Fine structuring

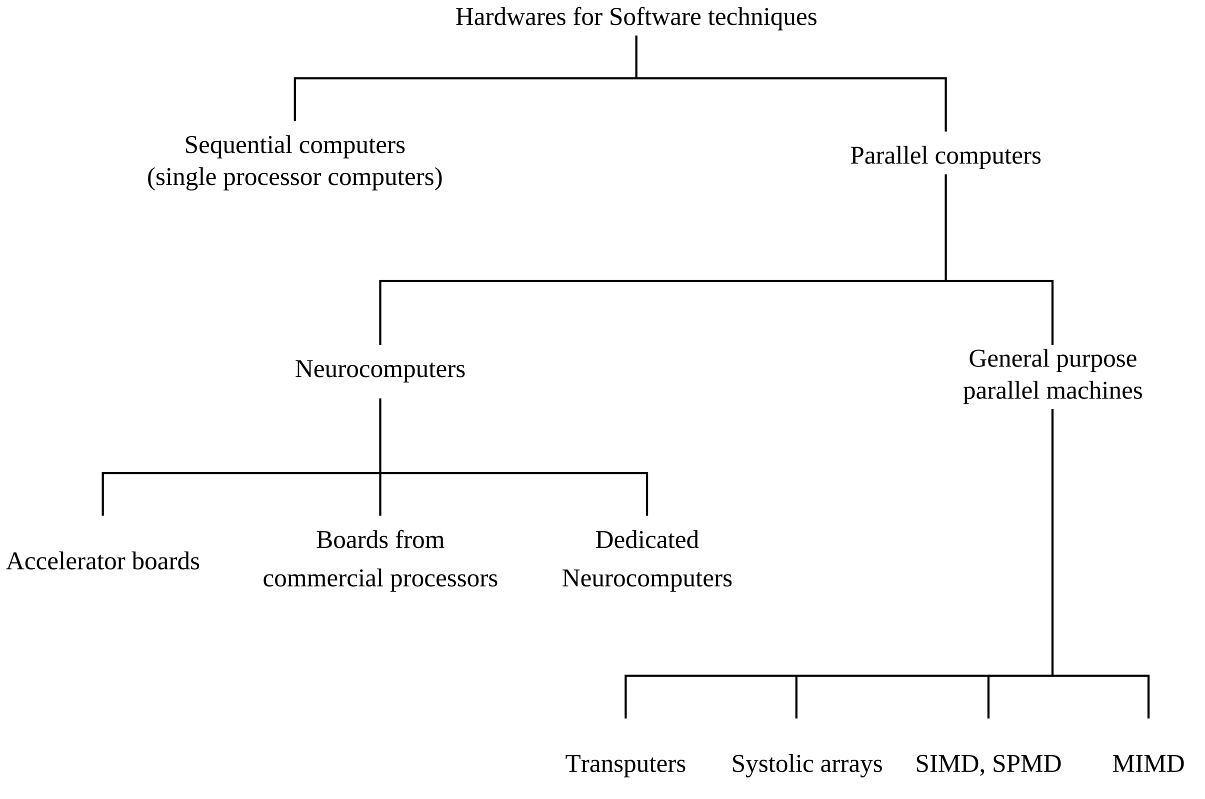




Parallel Implementations on General Purpose Machines

Structuring technique	Machine	**No. of proc.**	Benchmark	**Performance**
Coarse: training, node per layer	Connection Machine	64k	NetTalk	180M CPS, 38M CUPS
Coarse: training, node per layer	MasPar	16k	NetTalk	176M CPS, 42M CUPS
Fine: node, weight	Connection Machine	64k	NetTalk	13M CUPS
Pipeline: training, layer	Warp	10	NetTalk	17M CUPS
Pipeline: layer, node	Systolic array	13k	NetTalk	248M CUPS
Control parallel	Transputer	6		207k CUPS

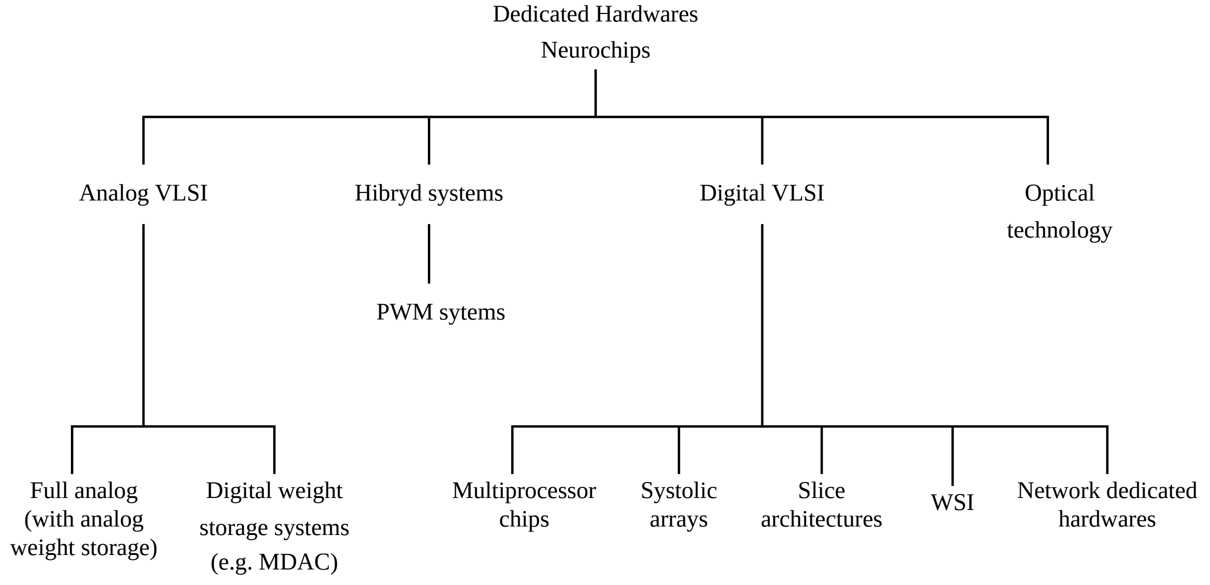
Hardware for Software Implementations



Computers for neuro-implementations should have some properties, like:

1. considerable **computational power**
2. sufficient **capacity** for large scale networks
3. sufficient **flexibility** for various network type
4. potential to implement new models

Dedicated Neuro-hardware, Neurochips


Dedicated Hardwares
Neurochips
Analog VLSI
Hibryd systems
Digital VLSI
Optical technology
PWM sytems
Full analog (with analog weight storage)
Digital weight storage systems (e.g. MDAC)
Multiprocessor chips
Systolic arrays
Slice architectures
WSI
Network dedicated hardwares

Analog Contra Digital Implementations

Advantages of analog implementation:

- High density
- Very high operating speed

Disadvantages of analog implementation

- Low precision
- Difficult implementation of variable weights
- Lack of adaptivity
- Hard to cascade chips
- Susceptibility
- Expensive fabrication
- Tricky to design

Analog Contra Digital Implementations

Advantages of digital implementation

- Arbitrary precision and dynamic range
- Flexibility
- Stability
- Insensitivity
- Relative small design experience is necessary

Disadvantages of digital implementation

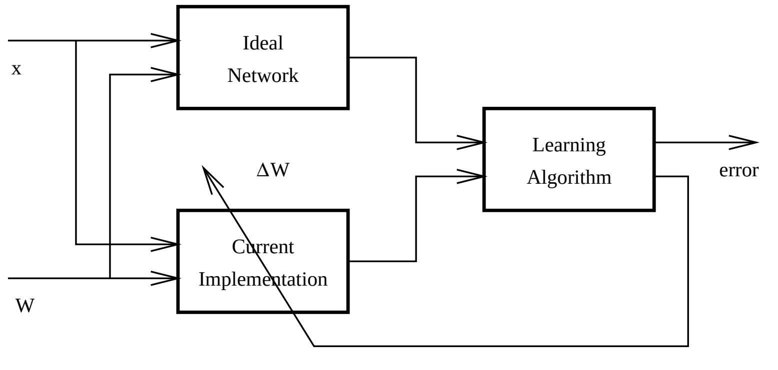
- Large required chip surface
- Lower operation speed

Benchmarking, Performance Criteria

Speed criteria

– CPS, Connections Per Second
– CUPS, Connection Update Per Second
– CPSPW, CPS Per Weight
– CUPSPW, CUPS Per Weight
– CPPS, Connection Primitives Per Second
– CPPS, Connection Primitives Per Second
– ECPPS, Effective Connection Primitives Per Second

Accuracy criteria

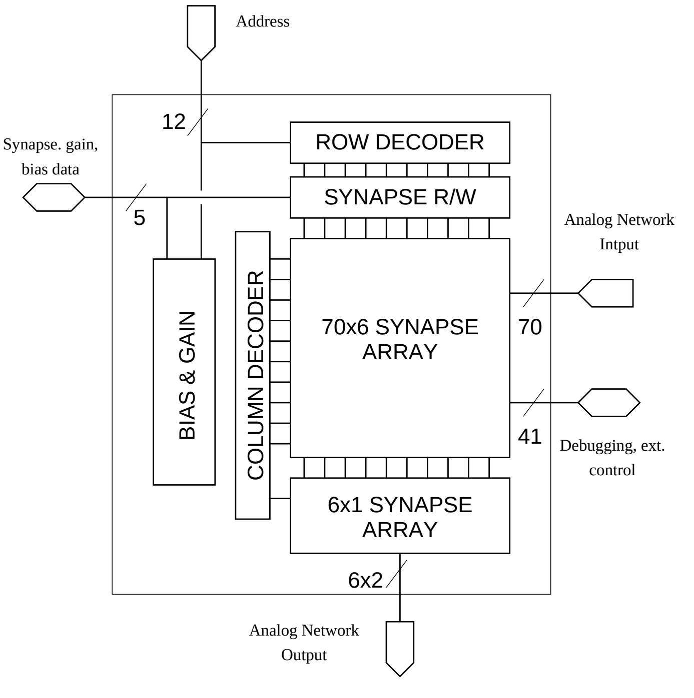


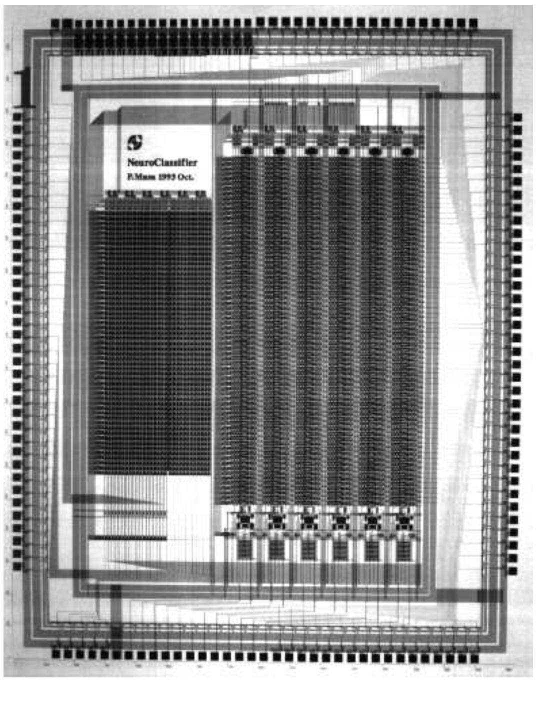
Criteria for size and reconfigurability

– Number of neurons per chip
– Number of weights per chip
– Connection Per Neuron
– Reconfigurability Number

Typical Implementation Examples, Analog Neurochips

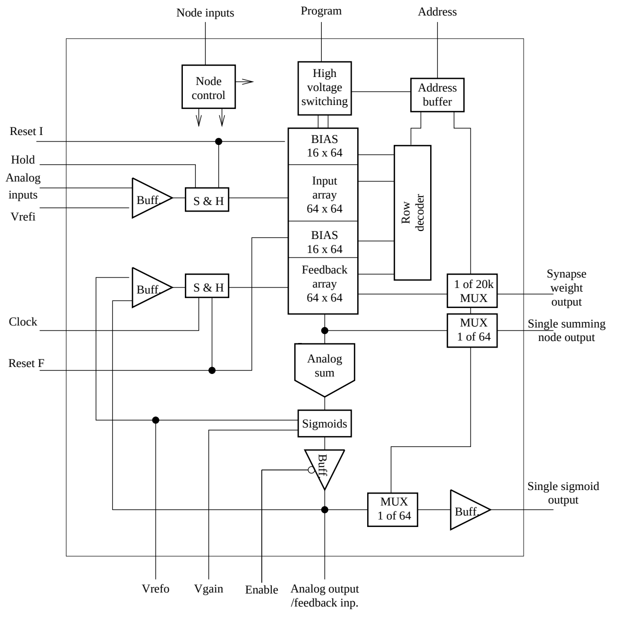
NeuroClassifier



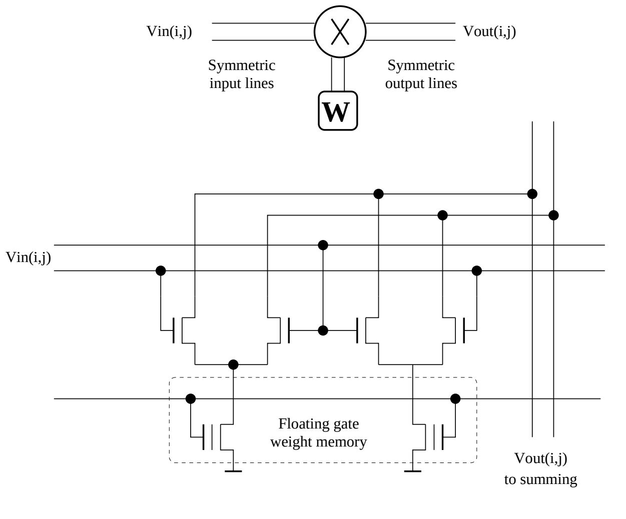


Typical Implementation Examples, Analog Neurochips

Intel ETANN chip



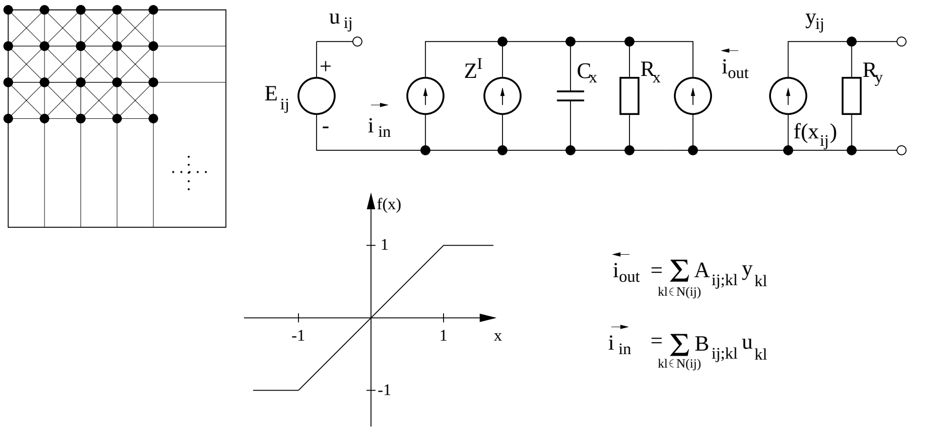
Block diagram of the ETANN chip



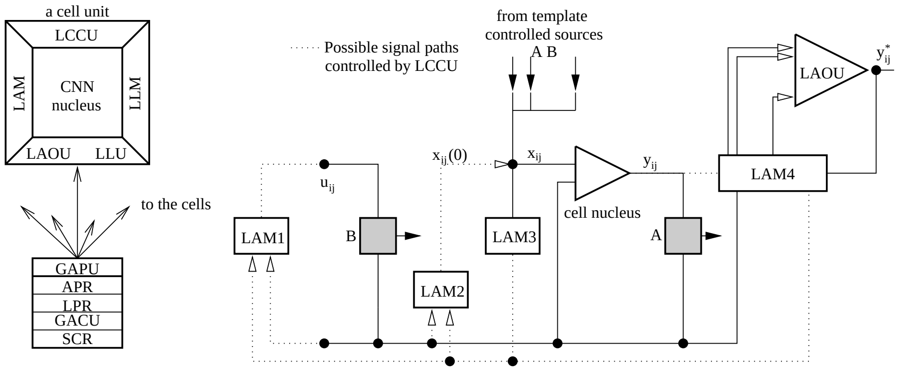
ETANN synapse implementation

Typical Implementation Examples, Analog Neurochips

CNN chip



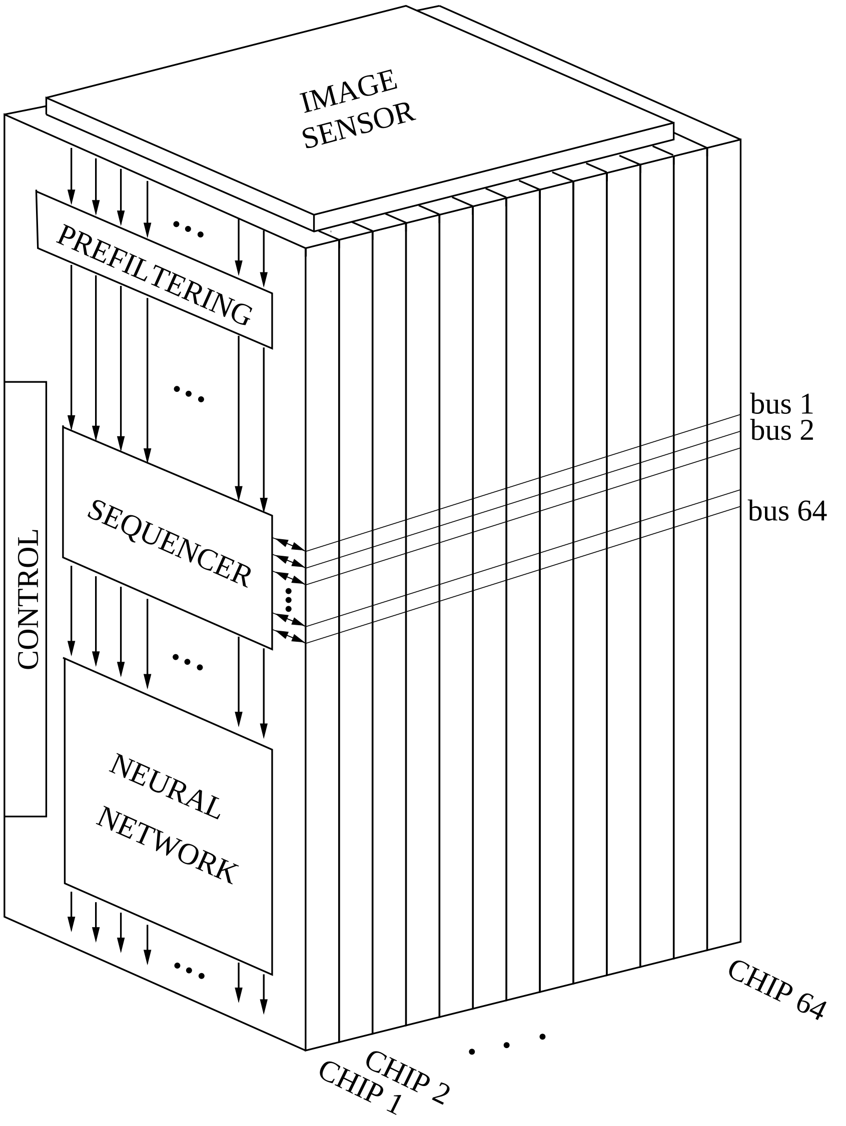
2-D CNN lattice and the circuit diagram of a simple CNN cell



Architecture of the CNN universal machine

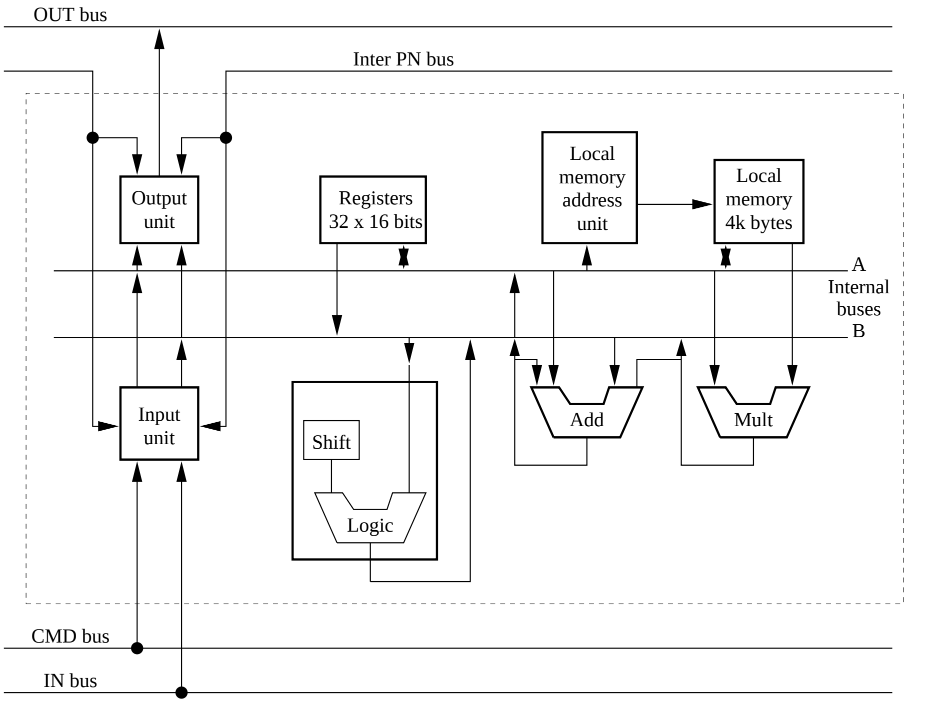
Typical Implementation Examples, Analog Neurochips

3-D IC stack analog neuroprocessor

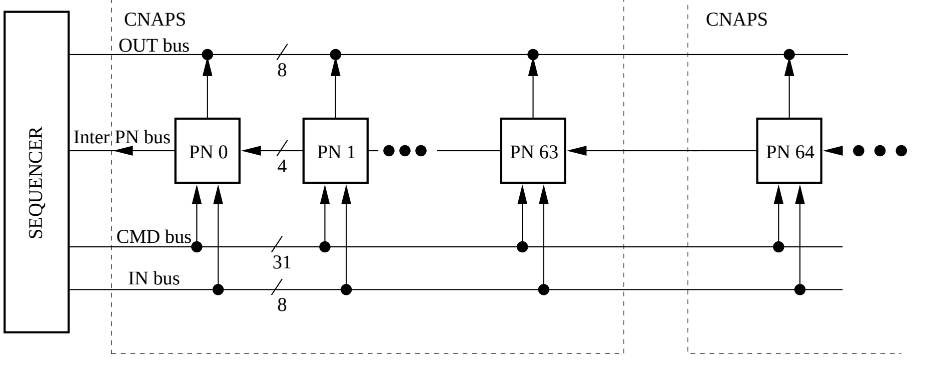


Typical Implementation Examples, Digital Neurochips

CNAPS (X1) SIMD multiprocessor chip



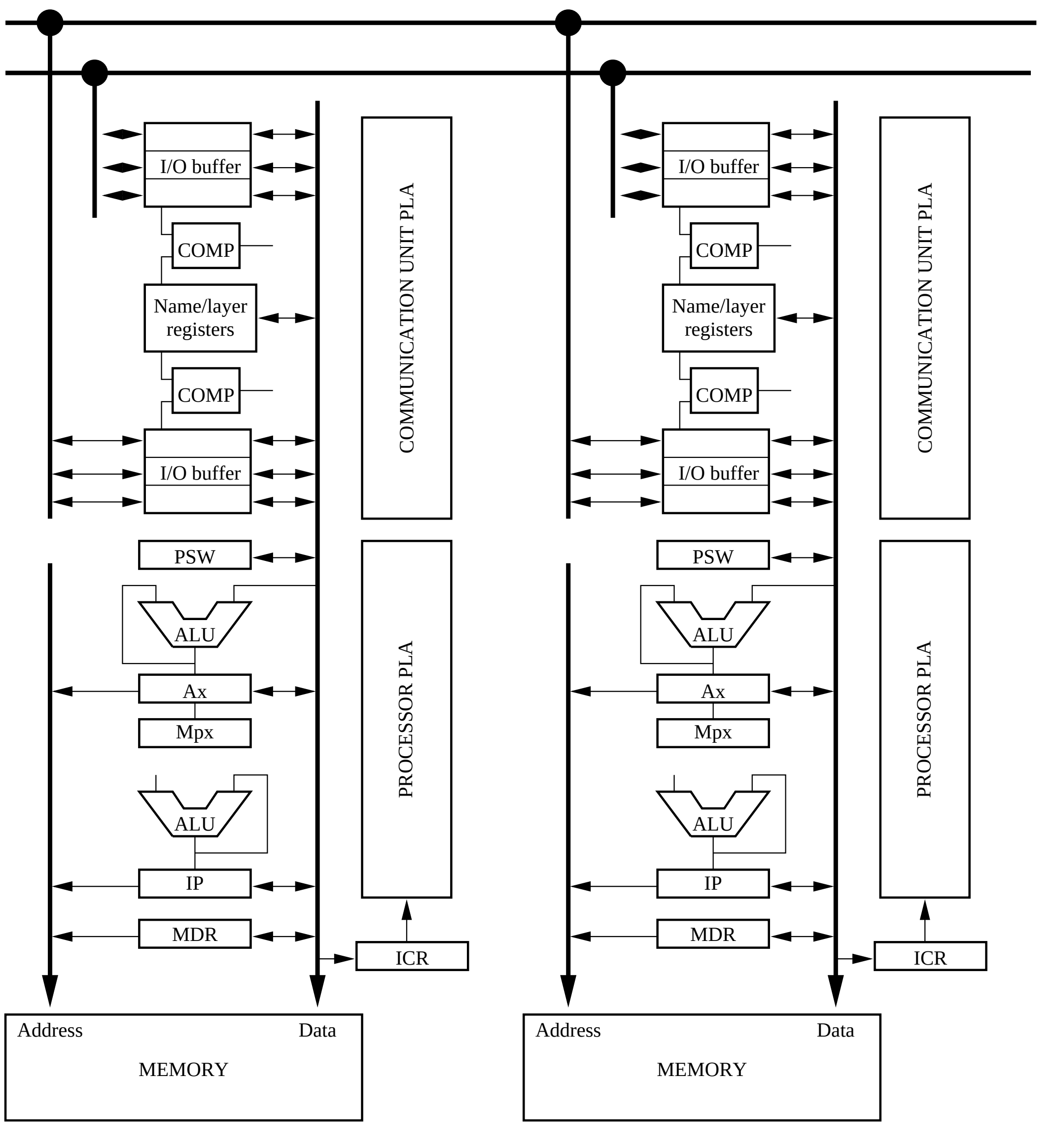
X1 chip



X1 chip array

Typical Implementation Examples, Digital Neurochips

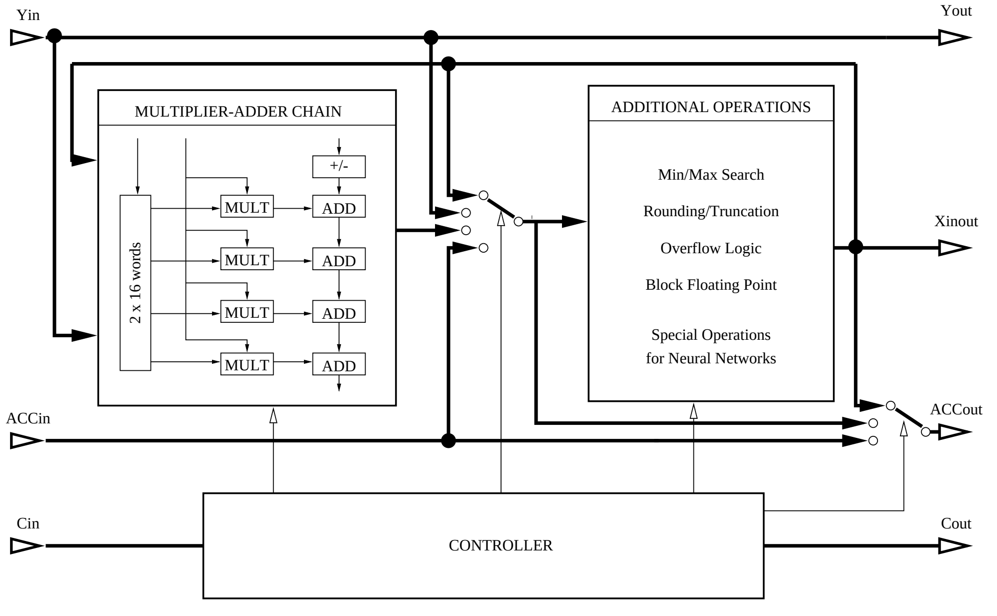
Neural RISC MIMD chip



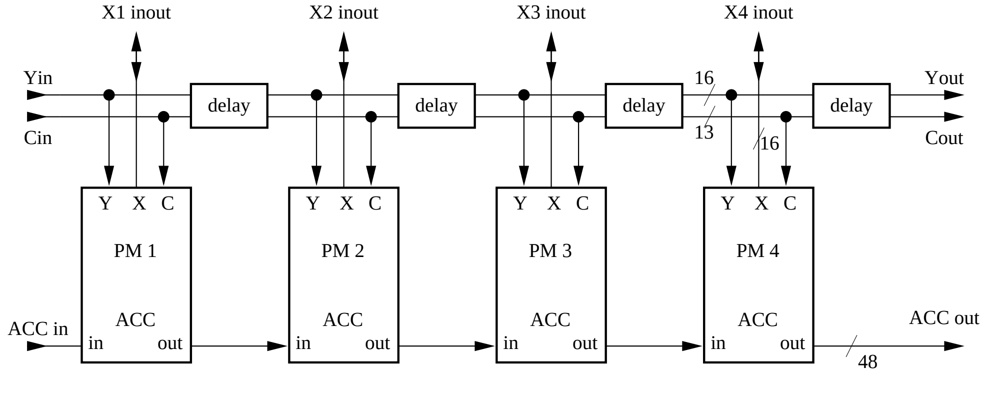
X1 chip

Typical Implementation Examples, Digital Neurochips

MA16 systolic array



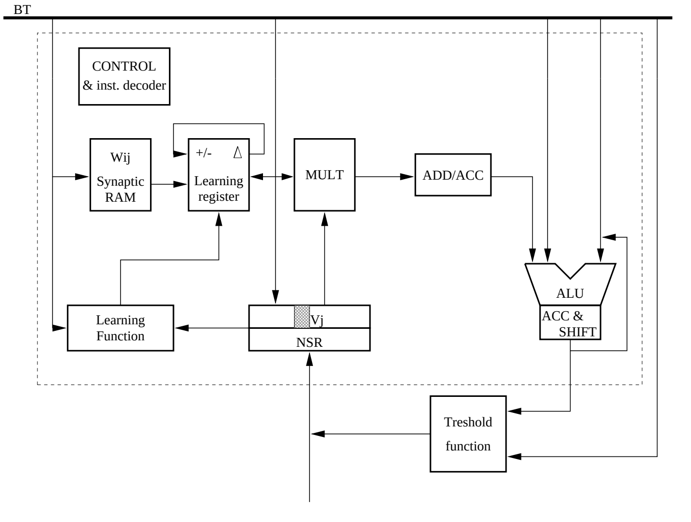
Block diagarm of a processor module



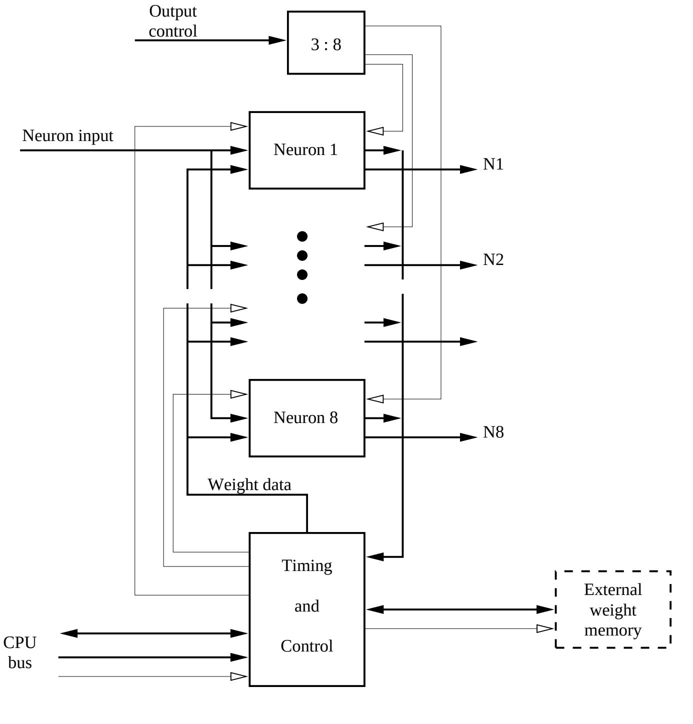
A systolic array of four PMs forms an MA16

Typical Implementation Examples, Digital Neurochips

Lneuro 1.0

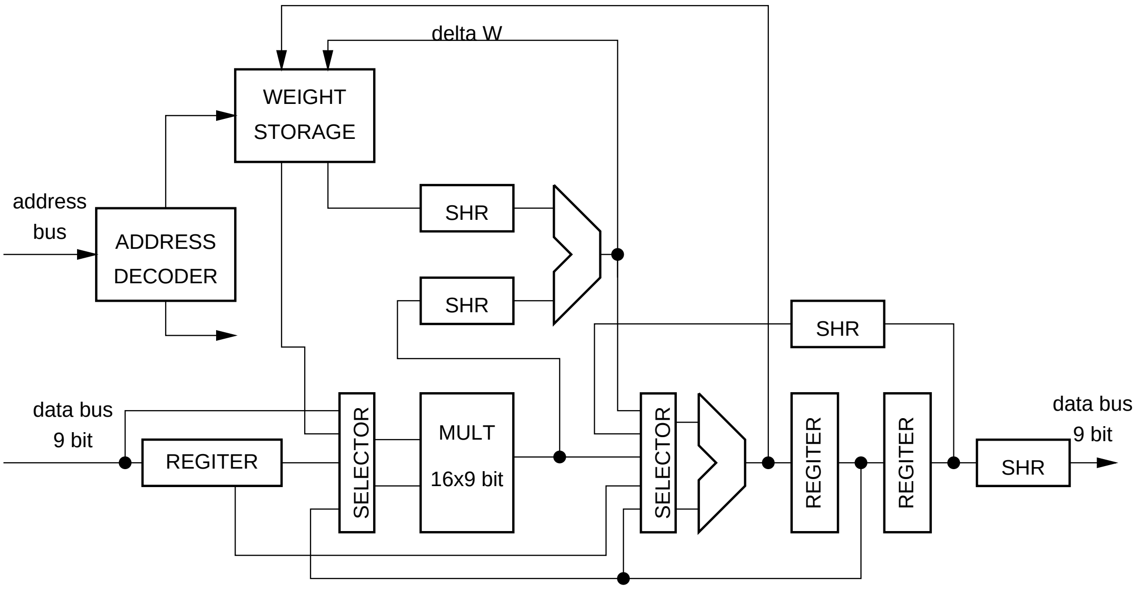


MD1220 Neural Bit Slice chip



Typical Implementation Examples, Digital Neurochips

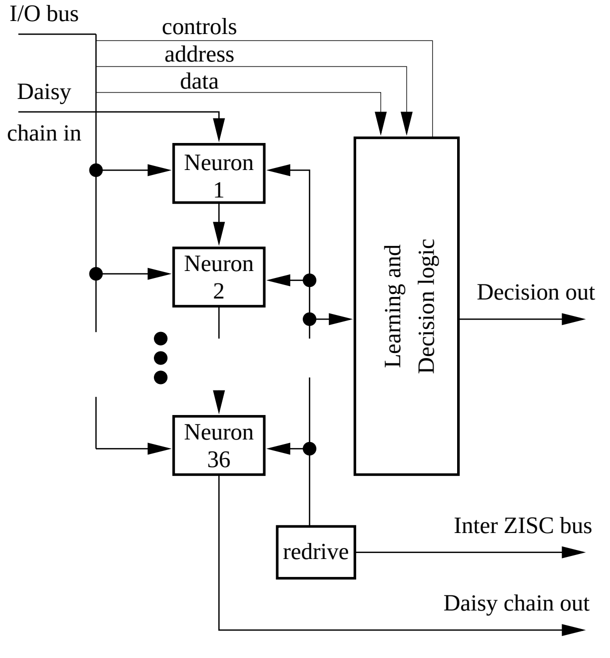
Hitachi Waffer Scale Integration (WSI) chip



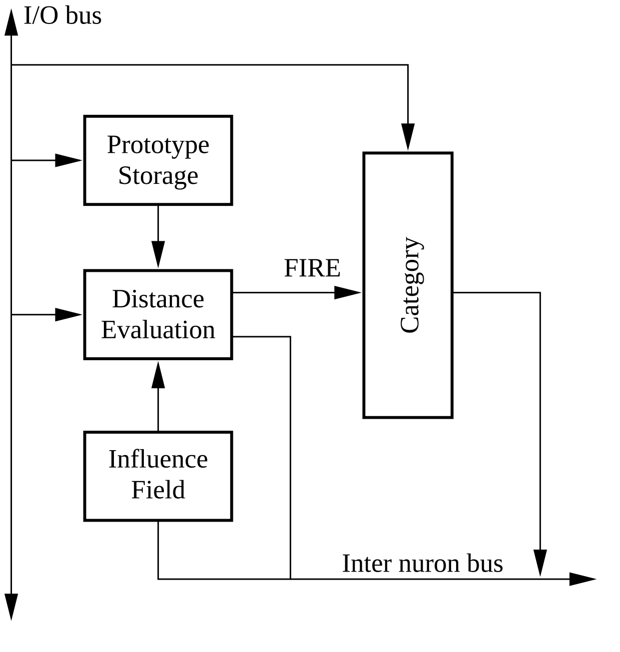
Block diagram of a neuron

Typical Implementation Examples, Digital Neurochips

ZISC RBF network dedicated chip



Block diagram of the ZISC036



Block diagram of a neuron

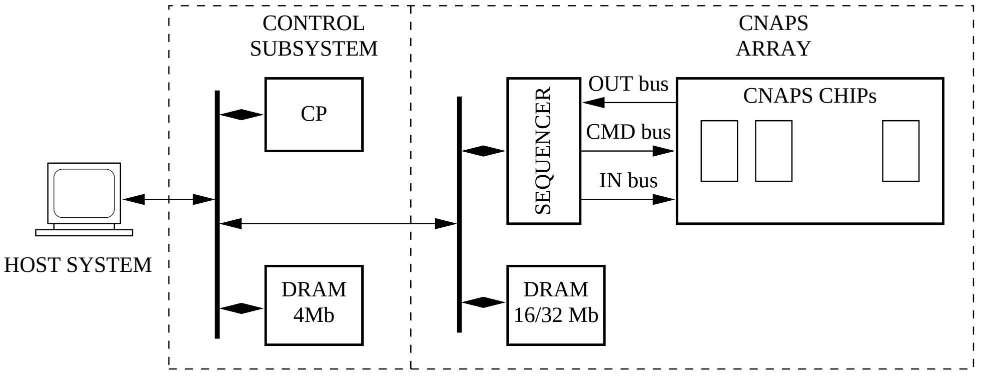
Typical Implementation Examples, Other Neurochips

Name	Type	Performance	Notes
Analog chips			
Synaptics Silicon Retina	Neuromorphic, analog	na	
Digital chips			
Neuralogix NLX-420	FdFwd, ML	300CPS	1-16bit, off-chip synapses
HNC 100-NAP	SIMD	250MCPS, 64MCUPS	100PE, 512k off-chip synapses
Inova N64000	SIMD	870MCPS, 220MCUPS	64PE, 128k synapses, 1-16bit
Nestor/Intel NI1000	RBF	40k pat./s, 27G CPS	1PE, 5bit
Accurate Aut. Corp. NNP	MIMD	140MCP	16bit
INCO SNAD/1	FdFwd, RBF	200MCPS	16bit mult., 40 bit add.
MT19003	FdFwd, ML	32MCPS	1x16bit, 1PE
TOTEM	SIMD	1G CPS	8x16bit, 32 MACC processors
Hybrid chips			
AT&T ANNA	FdFwd, ML	2.1GCPS	16-256 neurons, 3x6bit, 4k synapses
Bellcore CLNN-32	Boltzmann	100MCPS, 100MCUPS	6x5bit, 992 synapses
Ricoh RN-200	FdFwd, ML, BP	3GCPS	16 neurons, 256 synapses

Comparisation table of some other neurochips

Typical Implementation Examples, Neurocomputers Built from Neurochips

CNAPS



	CNAPS64	**CNAPS128**	**CNAPS256**	**CNAPS512**
Number of PNs	**64**	**128**	**256**	**512**
Total PN Memory (Each PN has 4k bytes) 1 Bit 8 Bit 16 Bit	 2M Bits 256k bytes 128k bytes	 4M Bits 512k bytes 256k bytes	 8M Bits 1M bytes 512k bytes	 16M Bits 2M bytes 1M bytes
Peak Performance MACC BP recall, CPS BP learning, CUPS	 960M 871M 220M	 1.92G 1.7G 429M	 3.84G 3.16G 813M	 7.68G 5.70G 1.46G

Performance of CNAPS systems

Typical Implementation Examples, Neurocomputers Built from Neurochips

CNAPS

Some software packages for CNAPS:

- *BuildNet* is an experimentation and application development package that offers some precoded neural algorithms

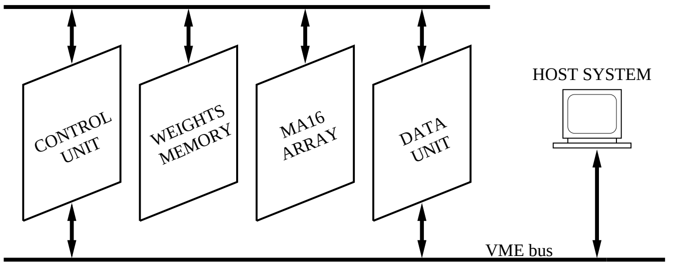
- *CodeNet* is an application development package to support custom neural algorithm development in CNAPS assembly

- *CNAPS-C* is a specialized parallel C compiler for CNAPS

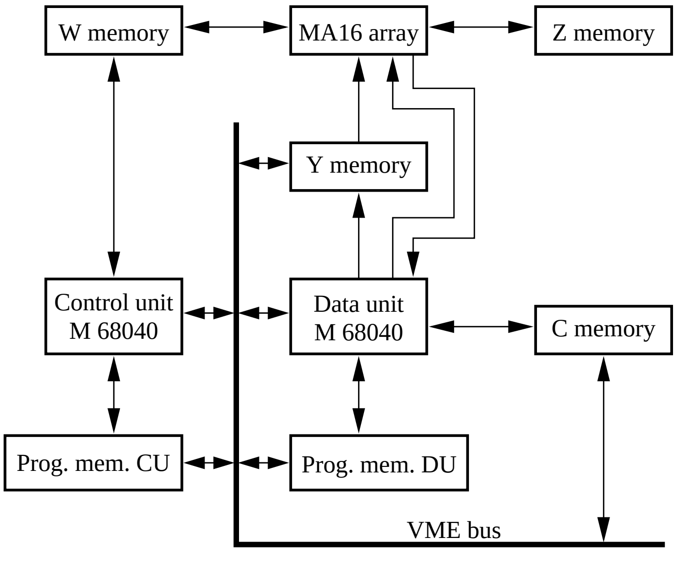
- *CNAPS Quicklib* is precoded function library for achiving maximum performance on CNAPS

Typical Implementation Examples, Neurocomputers Built from Neurochips

SYNAPSE-1



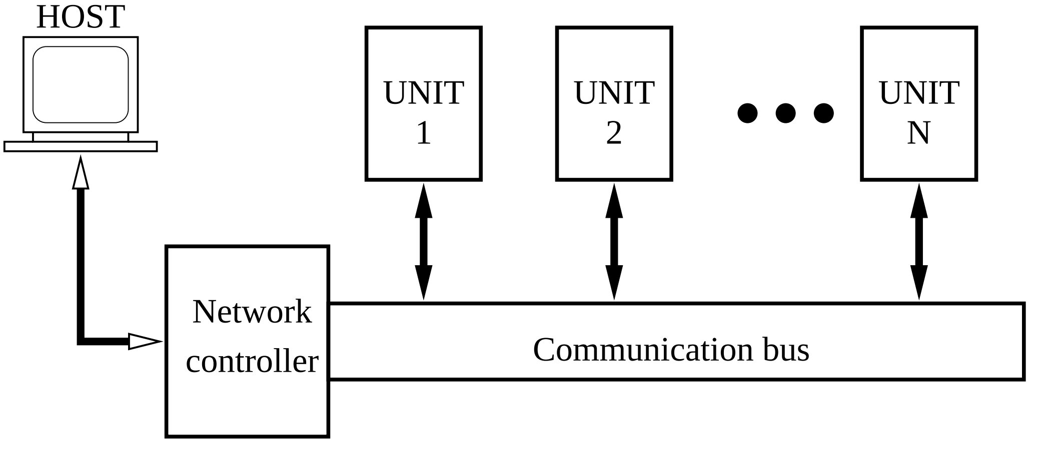
Block diagram of SYNAPSE-1



Processor memory architecture and data pathes

Typical Implementation Examples, Neurocomputers Built from Commercial Processors

BSP 400



Typical Implementation Examples, Other Neurocomputers

Name	Chip	Performance	Notes
Bellcore VME cascadable card	3 ETANN		
ETANN card, Bologna	ETANN, M68070		
RAP, Berkley	4-40 TMS320C40	57M CPS, 13.2M CUPS per board	VME bus
Texas, NETSIM	80188	450M CPS, 90M CUPS	15 cards, 256 neuron with 256 synapses each per board
REMAP, Luleåa Univ.	FPGAs	100-1G CPS	bit serial SIMD

Comparisation table of some other neurocomputers

Name	Chip	Performance	Notes
Current Tech. MM32k	spec. SIMD	4.9M CPS, 2.5M CUPS	
HNC Balbo 860	i860	80MFLOPS	
Neural Tech. NT6000	TMS320C20, MT19003	2M CPS	
NeurodynamX XR50	i860	45M CPS	
Sundance, SMT306	2 MT19003	2x 40M CPS	

Comparisation table of some other accelerator boards