

**SN820X**

**Internal  
Control**

**Application Note**

## Revision History

Revision	Date	Author	Change Description
1.1	Sept. 20, 2013	RF PD Department	Initial Release
1.2	June 10, 2014	R Willett	Reformatted in accordance with new Murata VI

---

This page intentionally left blank.

---

## Table of Contents

<b>1</b>	<b>SCOPE OF THE DOCUMENT .....</b>	<b>4</b>
<b>2</b>	<b>SN8200/SN8200UFL INTERNAL CONNECTION .....</b>	<b>4</b>
2.1	STM32F103RF - BRCM43362 Connection .....	4
2.2	Signal pin-outs .....	5
<b>3</b>	<b>SN8205/SN8205UFL INTERNAL CONNECTION .....</b>	<b>6</b>
3.1	STM32F205RG - BRCM43362 Connection .....	6
3.2	Signal pin-outs .....	6
<b>4</b>	<b>TECHNICAL SUPPORT CONTACT .....</b>	<b>7</b>

### LIST OF TABLES

Table 1:	SN8200 Wi-Fi Network Controller Module Family Configuration Comparison .....	4
Table 2:	SN8200 vs WICED SDK control .....	4
Table 3:	SN8200 Module signal description .....	5
Table 4:	SN8205 vs WICED SDK control .....	6
Table 5:	SN8205 module signal description .....	6

# 1 Scope of the Document

This document describes the complete pin assignments and STM32-BRCM43362 interface control for the SN820X module.

This application note applies to following SN820X modules.

Model #	P/N	Built-in STM	RAM Size	Flash Size
SN8200	88-00151-00	STM32F103RFT6TR	96KB	768KB
SN8200UFL	88-00151-02	STM32F103RFT6TR	96KB	768KB
SN8205	88-00158-00	STM32F205RGT6TR	128KB	1024KB
SN8205UFL	88-00158-02	STM32F205RGT6TR	128KB	1024KB

Table 1: SN8200 Wi-Fi Network Controller Module Family Configuration Comparison

## 2 SN8200/SN8200UFL Internal Connection

### 2.1 STM32F103RF - BRCM43362 Connection

SN8200 embodies the WICED architecture using the STM32F103RF Cortex M3 microcontroller and the BRCM43362 WiFi SoC. The interconnections between the two chips are the same as the reference WICED SDK with the following exceptions:

- The WiFi reset and LDO enable signals are PC1 and PC2 instead of PB5 and PB2
- WiFi LDO enable (WIFI\_VDD\_EN) is active high for SN8200, but it is active low for the WICED SDK.

WICED Signal	SN8200	WICED SDK
WL_RST_n	PC1	PB5
WIFI_VDD_EN	PC2	PB2

Table 2: SN8200 vs WICED SDK control

## 2.2 Signal pin-outs

The pin-outs for the module and the associated STM32F103RF values are described below in Table 3.

Pin	Pin name	STM32F103RF pin
5	ADC3	PA0/WKUP/ADC123_0/USART2_CTS TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR
6	ADC4	PA1/ADC123_1/USART2_RTS TIM2_CH2 / TIM5_CH2
7	ADC5	PA2/ADC123_2/USART2_TX TIM2_CH3 / TIM5_CH3 / TIM9_CH1
9	ADC6	PA3/ADC123_3/USART2_RX TIM2_CH4 / TIM5_CH4 / TIM9_CH2
10	DAC2	PA4/ADC12_4/DAC1/USART2_CK/SPI1_NSS
11	DAC1	PA5/ADC12_5/DAC2/SPI1_SCK
12	ADC1	PA7/ADC12_7/SPI1_MOSI
32	UART_TX	PA9/UART1_TX
33	UART_RX	PA10/UART1_RX
34	UART_CTS	PA11/UART1_CTS/USB2_DM/CAN_RX
35	UART_RTS	PA12/UART1_RTS/USB2_DP/CAN_TX
36	JTMS	PA13/JTMS/SWIO
37	JTDI/SPI_NSS	PA15/JTDI/SPI3_NSS/I2S3_WS
38	JTCK	PA14/JTCK/SWCLK
40	JTDO/SPI_SCK	PB3/JTDO/SPI3_SCK/I2S3_CK
41	JTRST/SPI_MISO	PB4/JTRST/SPI3_MISO
42	SPI_MOSI	PB5/I2C1_SMBA/SPI3_MOSI/ I2S3_SD
43	I2C_SCL	PB6/I2C1_SCL TIM4_CH1
44	I2C_SDA	PB7/I2C1_SDA TIM4_CH2
46	ADC2	PA6/ADC12_6/SPI1_MISO

**Table 3: SN8200 Module signal description**

## 3 SN8205/SN8205UFL Internal Connection

### 3.1 STM32F205RG - BRCM43362 Connection

SN8205/SN8205UFL embodies the WICED architecture using the STM32F205RG Cortex M3 microcontroller and the BRCM43362 WiFi SoC. The interconnections between the two chips are the same as the reference WICED SDK with the following exceptions:

- The WiFi reset and LDO enable signals are PC1 and PC2 instead of PB5 and PB2
- WiFi LDO enable (WIFI\_VDD\_EN) is active high for SN8205, but it is active low for the WICED SDK.

WICED Signal	SN8205	WICED SDK
WL_RST_n	PC1	PB5
WIFI_VDD_EN	PC2	PB2

Table 4: SN8205 vs WICED SDK control

### 3.2 Signal pin-outs

The pin-outs for the module and the associated STM32F205RG values are described below in Table 5.

Pin	Pin name	STM32F103RF pin
5	ADC3	PA0/WKUP/ADC123_0/USART2_CTS TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR
6	ADC4	PA1/ADC123_1/USART2_RTS TIM2_CH2 / TIM5_CH2
7	ADC5	PA2/ADC123_2/USART2_TX TIM2_CH3 / TIM5_CH3 / TIM9_CH1
9	ADC6	PA3/ADC123_3/USART2_RX TIM2_CH4 / TIM5_CH4 / TIM9_CH2
10	DAC2	PA4/ADC12_4/DAC1/USART2_CK/SPI1_NSS
11	DAC1	PA5/ADC12_5/DAC2/SPI1_SCK
12	ADC1	PA7/ADC12_7/SPI1_MOSI
32	UART_TX	PA9/UART1_TX
33	UART_RX	PA10/UART1_RX
34	UART_CTS	PA11/UART1_CTS/USB2_DM/CAN_RX
35	UART_RTS	PA12/UART1_RTS/USB2_DP/CAN_TX
36	JTMS	PA13/JTMS/SWIO
37	JTDI/SPI_NSS	PA15/JTDI/SPI3_NSS/I2S3_WS
38	JTCK	PA14/JTCK/SWCLK
40	JTDO/SPI_SCK	PB3/JTDO/SPI3_SCK/I2S3_CK
41	JTRST/SPI_MISO	PB4/JTRST/SPI3_MISO
42	SPI_MOSI	PB5/I2C1_SMBA/SPI3_MOSI/ I2S3_SD
43	I2C_SCL	PB6/I2C1_SCL TIM4_CH1
44	I2C_SDA	PB7/I2C1_SDA TIM4_CH2
46	ADC2	PA6/ADC12_6/SPI1_MISO

Table 5: SN8205 module signal description

---

## 4 Technical Support Contact

Contact Wireless module application support at [modules@murata.com](mailto:modules@murata.com)

Murata Electronics, N.A., Inc.

4441 Sigma Road

Dallas, TX 75244

USA