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SN82XX

EV Board

Application Note

Revision History

Revision	Date	Author	Change Description
V1.0	2/26/2013	RF PD Department	Initial version
V1.1	9/20/2013	RF PD Department	Added support to all SN820X
V2.0	06-10-2014	R Willett	Reformatted to comply with new Murata VI

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1 Scope

This document is a supplementary note to the SN820X SNIC EVK+ User Guide to provide guidance on how to use the SN820X Wi-Fi module EV Board to download the firmware to separate module and how to connect the EV Board to customer host board for software development.

This application note applies to following SN820X EVKs.

Model #	P/N
SN8200 EVK+	88-00151-95
SN8200UFL EVK+	88-00151-97
SN8205 EVK+	88-00158-95
SN8205UFL EVK+	88-00158-97

Table 1: List of applicable EVKs

2 Purpose

1. The SN82XX EVB can be used as temporary firmware downloading tool. This document addresses the hardware configuration for this purpose.
2. The SN820X EVK+ is also a software development tool for host platform software programming. This document addresses the hardware connection for this purpose.

3 SN82XX EV Board as a firmware flash tool

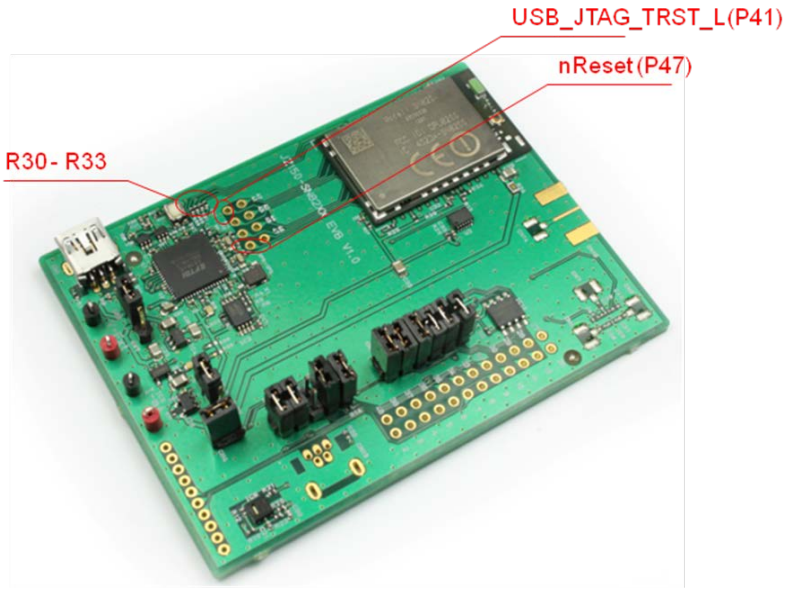

Figure 1: SN82XX EVB

The SNIC Monitor uses the FTDI USB-JTAG to download the FW. The customer needs to reroute the JTAG pins to connect the JTAG pins from the FTDI chip to the module that will be flashed.

1. Remove zero ohm resistors R30, R31, R32, and R33. Connect those FTDI signals to the corresponding JTAG_TCK, TDI, TDO, TMS pins of the new SN820X module.
2. Connect USB_JTAG_TRST_L (P41) to the corresponding pin of the new SN820X.
3. Connect nRESET (p47) to nRESET of the new SN820X

The EVB schematic is in SNIC\Documents\SN82XX EVB JZ150 SCH.pdf.

4 Connect the EV Board to host UART interface

The SN820X module on the SN82XX EVB can be isolated and directly connected to a host platform. When connect to the customer target board, the following hardware modifications is needed to allow the host CPU/MCU to control the SN820X directly using the SNIC UART serial interface.

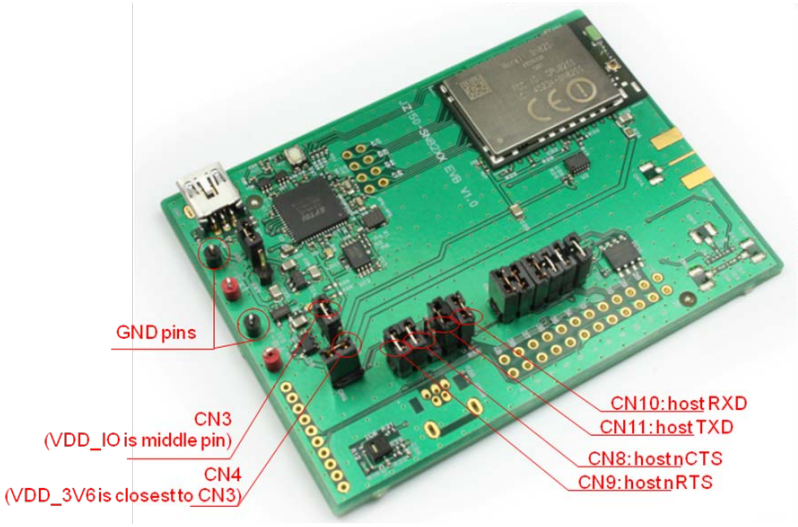

Figure 2: Configuration of SN82XX EVB to Host UART

1. Configure and download the FW to SN820X using the SNIC Monitor through USB
2. Remove jumpers from CN8, CN9, CN10 and CN11 to disconnect the FTDI UART path to SN820X. The SNIC Monitor will no longer be functional from this point except for firmware downloading.
3. Connect the SN820X UART pins to the corresponding pins in the host platform as shown in Figure 2. The host connection must be connected to the row of header pins closest to the right edge of the EVB and furthest from the module.
4. Connect GND of host platform to SN820X through one of the black GND pins.
5. Remove jumpers from CN3 and CN4. Connect VDD_IO (middle pin of CN3) and VDD_3V6 (pin closest to CN3) to the corresponding power rail of the host platform. If only a single power rail is available, then connect VDD_3V6 to the host power rail and select VDD_3V6 as VDD_IO by placing a jumper on the two CN3 pins closest to CN4.

The EVB schematic is in SNIC\Documents\SN82XX EVB JZ150 SCH.pdf.

5 Connect the EV Board to host SPI interface

The customer application communicates with the SN820X module via the SPI interface (up to 18MBits/s). In the SNIC application, the SN820X is the SPI slave. Since SN820X is the SPI slave, it requires the master to provide the clock to send data to the host controller. When the SN820X module has data, it indicates to the host by asserting a dedicated GPIO line (ALRT/). The signal transitions from high to low to signal the event, and returns to the high state prior to the completion of the current data transfer. If the host connects this signal to an interrupt line, then upon receiving the GPIO interrupt, the host may assert NSS and start clock to initiate data transfer from the module. In the case when the GPIO interrupt pin is not available on the host, it may assert NSS and send clock periodically to poll data from the module.

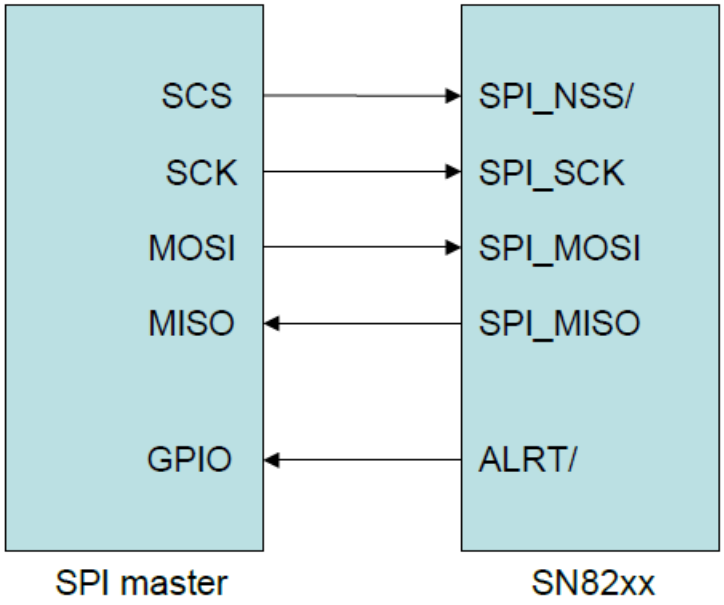

Figure 3: SN820X-host SNIC SPI interface diagram

The SN820X module on the SN82XX EVB can be isolated and directly connected to a host platform. When connect to the customer target board, the following hardware modifications is needed to allow the host CPU/MCU to control the SN820X directly using the SNIC SPI serial interface.

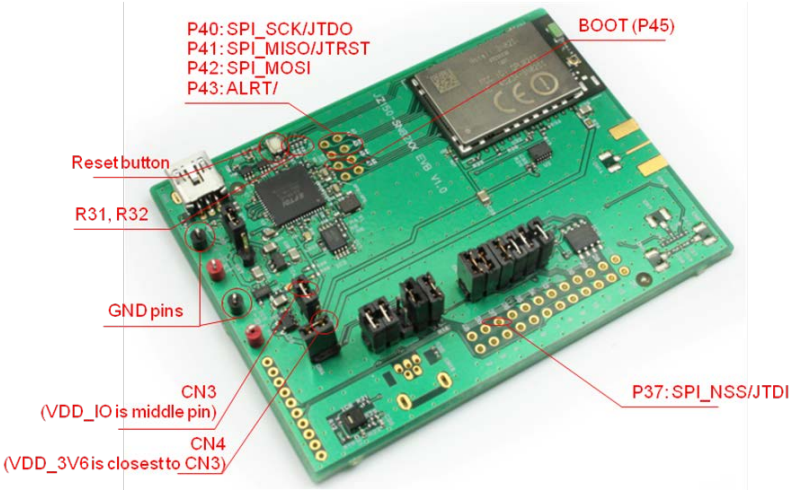

Figure 4: Configuration of SN82XX EVB to Host SPI

NOTE:

1. Configure and download the FW to SN820X using the SNIC Monitor through USB.

   The SPI interface shares 3 pins with the JTAG, so it is necessary to place SN820X into BOOT mode to disable the SPI interface before using the JTAG to download a new FW into SN820X. The following procedure may be used to down the new FW to the EVB:

   a) Pull BOOT high.

   b) Press and release Reset button.

   c) Download FW using JTAG.

   d) Remove pull-up on BOOT and press Reset.

2. Remove zero ohm resistors R31 and R32 to disconnect the FTDI JTAG from the SPI interface. The firmware download will no longer be functional from this point.
3. Connect the host IO to ALRT/ if that signal is used. By default, ALRT/ is P43.
4. Connect the SN820X SPI pins to the corresponding test pads in the host platform as shown in Figure 4.
5. Connect GND of host platform to SN820X through one of the black GND pins.
6. Remove jumpers from CN3 and CN4. Connect VDD_IO (middle pin of CN3) and VDD_3V6 (pin closest to CN3) to the corresponding power rail of the host platform. If only a single power rail is available, then connect VDD_3V6 to the host power rail and select VDD_3V6 as VDD_IO by placing a jumper on the two CN3 pins closest to CN4.

The EVB schematic is in SNIC\Documents\SN82XX EVB JZ150 SCH.pdf.

6 Technical Support Contact

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