AN4660
Application note

Migration of microcontroller applications from STM32F42xxx/F43xxx devices to STM32F7 Series devices

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on the memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require to switch to smaller components and to shrink the PCB area.

This application note analyzes the steps required to migrate from an existing STM32F42xxx/F43xxx device to a STM32F7 Series device based design.

This application note provides a guideline on the hardware migration and the peripheral migration. To fully benefit from this application note, the user should be familiar with the STM32 microcontroller family.

For additional information, refer to the following documents available on *www.st.com*:

- *STM32F405/415, STM32F407/417, STM32F427/437 and STM32F429/439 advanced ARM®-based 32-bit MCUs* reference manual *(RM0090)*
- *STM32F72xxx and STM32F73xxx advanced ARM®-based 32-bit MCUs* reference manual *(RM0431)*
- *STM32F75xxx and STM32F74xxx advanced ARM®-based 32-bit MCUs* reference manual *(RM0385)*
- *STM32F76xxx and STM32F77xxx advanced ARM®-based 32-bit MCUs* reference manual *(RM0410)*

Table 1. Applicable products

Type	Product lines and Series
Microcontrollers	STM32F427/437 line, STM32F429/439 line
	STM32F7 Series

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1 Hardware migration

1.1 Pinout compatibility

1.1.1 LQFP100 package

The STM32F74xxx/F75xxx/F76xxx/F77xxx/F7x2xx devices are fully pin-to-pin compatible with the STM32F42xxx/F43xxx devices except for the LQFP100 package, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

The STM32F7x3xx devices (x=2 or 3) are not compatible with the STM32F42xxx/F43xxx devices due to the USB PHY HS functionality on some pins.

In this application note, the pinout migration to the STM32F7x3xx product is not covered. In order to migrate to this product, refer to *Migration of microcontroller applications between STM32F74xxx/75xxx and STM32F72xxx/F73xxx* application note (AN4946).

Figure 1 and *Table 2* present the pinout differences between the STM32F42xxx/F43xxx and STM32F74xxx/F75xxx/F76xxx/F77xxx/F7x2xx devices for the LQFP100 package.

Figure 1. Incompatible board design for LQFP100 package

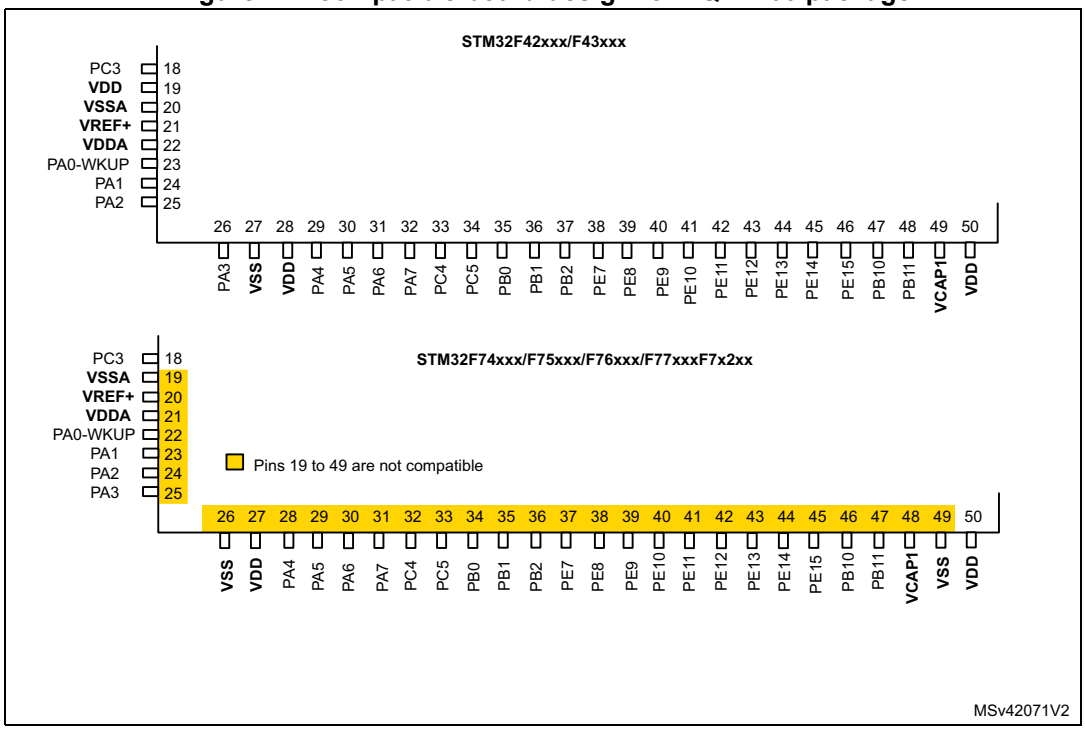


Table 2. STM32F42xxx/F43xxx and STM32F4xxx/F75xxx/F76xxx/F77xxx/F7x2xx pinout differences (LQFP100)

LQFP100	STM32F42xxx/F43xxx pinout	STM32F74xxx/F75xxx/ F76xxx/F77xxx/F76xxx/ F7x2xx pinout
19	VDD	VSSA
20	VSSA	VREF+
21	VREF+	VDDA
22	VDDA	PA0-WKUP
23	PA0-WKUP	PA1
24	PA1	PA2
25	PA2	PA3
26	PA3	VSS
27	VSS	VDD
28	VDD	PA4
29	PA4	PA5
30	PA5	PA6
31	PA6	PA7
32	PA7	PC4
33	PC4	PC5
34	PC5	PB0
35	PB0	PB1
36	PB1	PB2
37	PB2	PE7
38	PE7	PE8
39	PE8	PE9
40	PE9	PE10
41	PE10	PE11
42	PE11	PE12
43	PE12	PE13
44	PE13	PE14
45	PE14	PE15
46	PE15	PB10
47	PB10	PB11
48	PB11	VCAP1
49	VCAP1	VSS
53	PB14	PB14
54	PB15	PB15

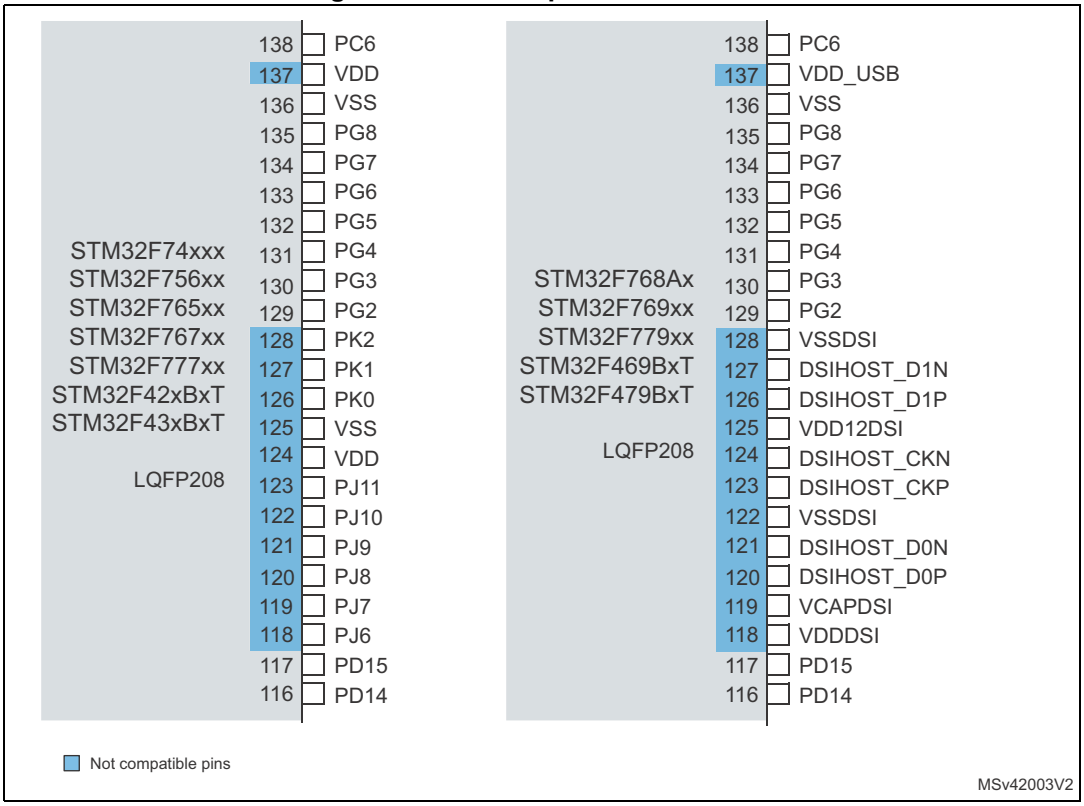
Table 2. STM32F42xxx/F43xxx and STM32F4xxx/F75xxx/F76xxx/F77xxx/F7x2xx pinout differences (LQFP100) (continued)

LQFP100	STM32F42xxx/F43xxx pinout	STM32F74xxx/F75xxx/ F76xxx/F77xxx/F76xxx/ F7x2xx pinout
55	PD8	PD8
56	PD9	PD9
57	PD10	PD10

1.1.2 LQFP208 package

Figure 2 and *Table 3* present the pinout differences between the STM32F74xxx/STM32F756xx/STM32F765xx/STM32F767xx/STM32F777xx/STM32F42xBxT/STM32F43xBxT and the STM32F768Ax/STM32F769xx/STM32F779xx/STM32F469BxT/STM32F479BxT devices for the LQFP208 package.

Figure 2. LQFP208 pinout differences



For the highlighted (blue) terminals, the DSIHOST dedicated IOs on the STM32F768Ax/STM32F769xx/STM32F779xx/STM32F469BxT/STM32F479BxT devices substitute some of STM32F74xxx/STM32F756xx/STM32F765xx/STM32F767xx/STM32F777xx/STM32F42xBxT/STM32F43xBxT IO ports.

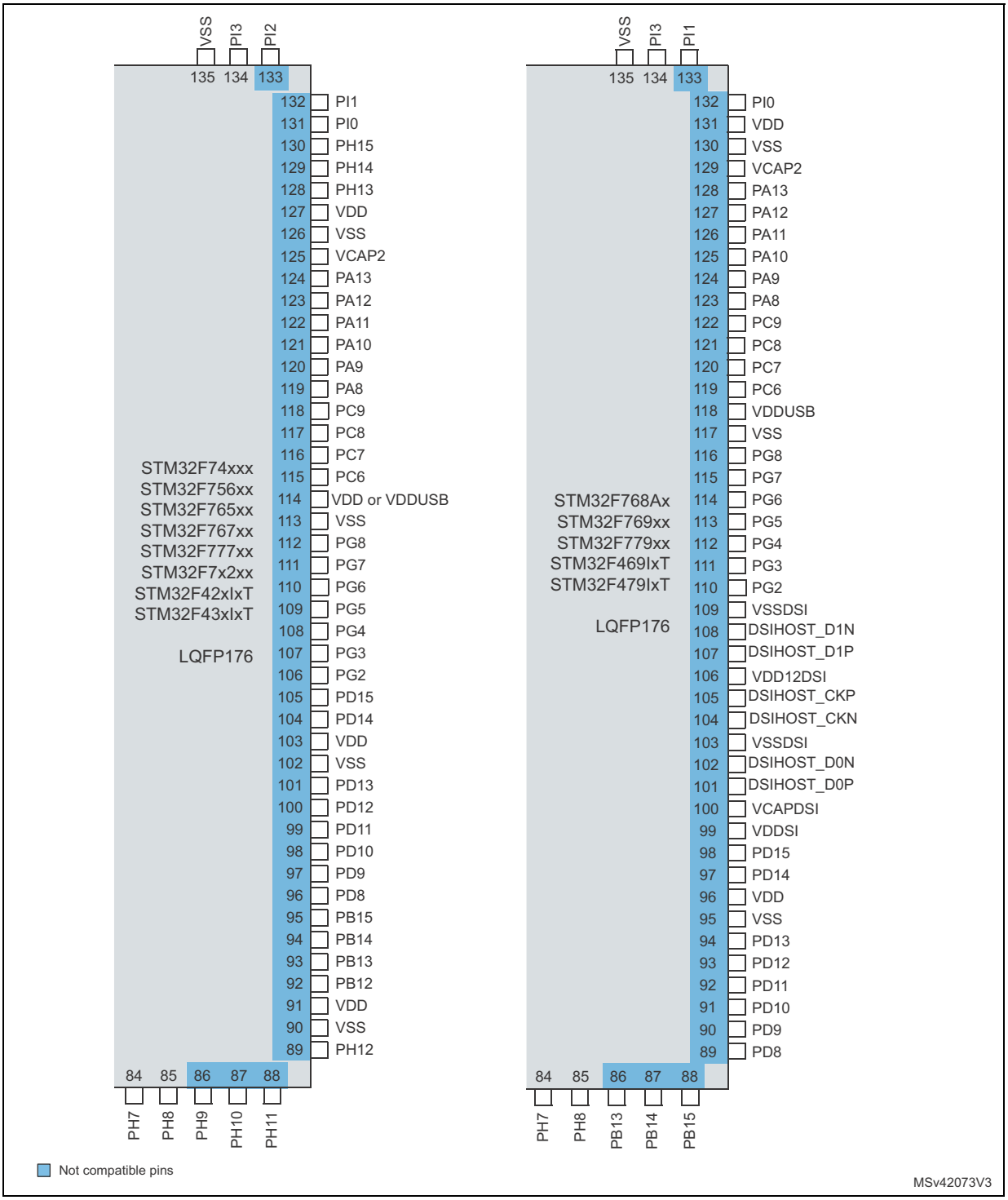
Table 3. List of LQFP208 pinout differences

Terminal	STM32F74xxx STM32F756xx STM32F765xx STM32F767xx STM32F777xx STM32F42xBxT STM32F43xBxT	STM32F768Ax STM32F769xx STM32F779xx STM32F469BxT STM32F479BxT	Terminal	STM32F74xxx STM32F756xx STM32F765xx STM32F767xx STM32F777xx STM32F42xBxT STM32F43xBxT	STM32F768Ax STM32F769xx STM32F779xx STM32F469BxT STM32F479BxT
128	PK2	VSSDSI	122	PJ10	VSSDSI
127	PK1	DSIHOST_D1N	121	PJ9	DSIHOST_D0N
126	PK0	DSIHOST_D1P	120	PJ8	DSIHOST_D0P
125	VSS	VDD12DSI	119	PJ7	VCAPDSI
124	VDD	DSIHOST_CKN	118	PJ6	VDDDSI
123	PJ11	DSIHOST_CKP	137	VDD	VDD_USB

1.1.3 LQFP176 package

Figure 3 and *Table 4* present the pinout differences between the STM32F74xxx/STM32F756xx/STM32F765xx/STM32F767xx/STM32F777xx/STM32F7x2xx /STM32F42xIxT/STM32F43xIxT and the STM32F768Ax/STM32F769xx/STM32F469IxT/STM32F479IxT devices for the LQFP176 package.

Figure 3. LQFP176 pinout differences



The highlighted (blue) terminals have different IO port assignment.

Table 4. List of LQFP176 pinout differences

Terminal	STM32F74xxx STM32F756xx STM32F765xx STM32F767xx STM32F777xx STM32F7x2xx STM32F42xIxT STM32F43xIxT	STM32F768Ax STM32F769xx STM32F779xx STM32F469IxT STM32F479IxT
133	PI2	PI1
132	PI1	PI0
131	PI0	VDD
130	PH15	VSS
129	PH14	VCAP2
128	PH13	PA13
127	VDD	PA12
126	VSS	PA11
125	VCAP2	PA10
124	PA13	PA0
123	PA12	PA8
122	PA11	PC9
121	PA10	PC8
120	PA9	PC7
119	PA8	PC6
118	PC9	VDDUSB
117	PC8	VSS
116	PC7	PG8
115	PC6	PG7
114	VDD or VDDUSB	PG6
113	VSS	PG5
112	PG8	PG4
111	PG7	PG3
110	PG6	PG2
109	PG5	VSSDSI
108	PG4	DSIHOST_D1N
107	PG3	DSIHOST_D1P
106	PG2	VDD12DSI
105	PD15	DSIHOST_CKP
104	PD14	DSIHOST_CKN

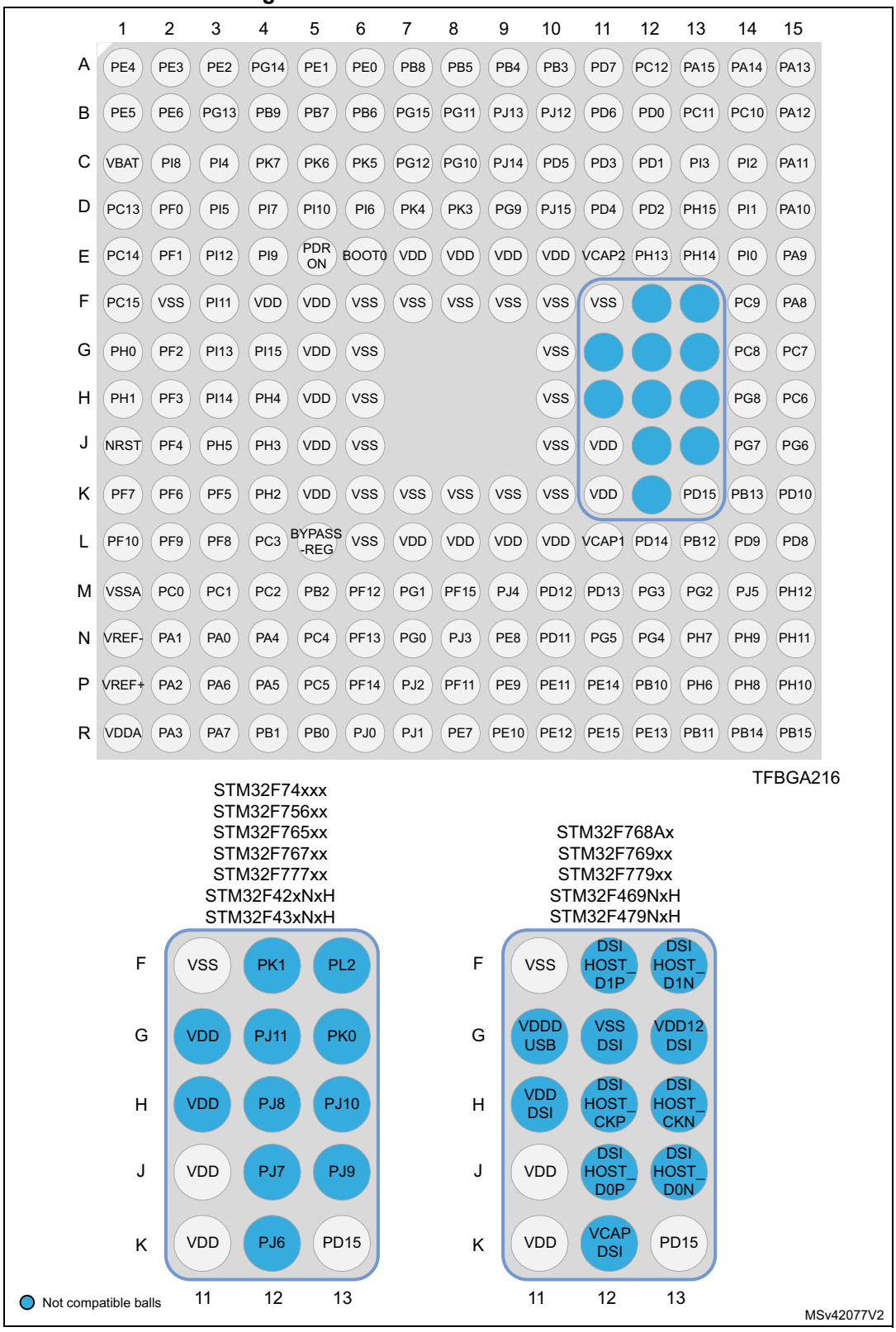
Table 4. List of LQFP176 pinout differences (continued)

Terminal	STM32F74xxx STM32F756xx STM32F765xx STM32F767xx STM32F777xx STM32F7x2xx STM32F42xIxT STM32F43xIxT	STM32F768Ax STM32F769xx STM32F779xx STM32F469IxT STM32F479IxT
103	VDD	VSSDSI
102	VSS	DSIHOST_D0N
101	PD13	DSIHOST_D0P
100	PD12	VCAPDSI
99	PD11	VDDDSI
98	PD10	PD15
97	PD9	PD14
96	PD8	VDD
95	PB15	VSS
94	PB14	PD13
93	PB13	PD12
92	PB12	PD11
91	VDD	PD10
90	VSS	PD9
89	PH12	PD8
88	PH11	PB15
87	PH10	PB14
86	PH9	PB13

1.1.4 TFBGA216 package

Figure 4 and *Table 5* present the ballout differences between the STM32F74xxx/STM32F756xx/STM32F765xx/STM32F767xx/STM32F777xx/STM32F42xNxH/STM32F43xNxH and the STM32F768Ax/STM32F769xx/STM32F469NxH/STM32F479NxH devices for the TFBGA216 package.

Figure 4. TFBGA216 ballout differences



For the highlighted (blue) terminals, the DSIHOST dedicated IOs on the STM32F768Ax/STM32F769xx/STM32F779xx/STM32F469NxH/STM32F479NxH devices substitute some of STM32F74xxx/STM32F756xx/STM32F765xx/STM32F767xx/STM32F777xx/ STM32F42xNxH/STM32F43xNxH IO ports.

Table 5. List of TFBGA216 ballout differences

Terminal	STM32F74xxx STM32F756xx STM32F765xx STM32F767xx STM32F777xx STM32F42xNxH STM32F43xNxH	STM32F768Ax STM32F769xx STM32F779xx STM32F469NxH STM32F479NxH	Terminal	STM32F74xxx STM32F756xx STM32F765xx STM32F767xx STM32F777xx STM32F42xNxH STM32F43xNxH	STM32F768Ax STM32F769xx STM32F779xx STM32F469NxH STM32F479NxH
11G	VDD	VDDDUSB	12K	PJ6	VCAPDSI
11H	VDD	VDDDSI	13F	PL2	DSIHOST_D1N
12F	PK1	DSIHOST_D1P	13G	PK0	VDD12DSI
12G	PJ11	VSSDSI	13H	PJ10	DSIHOST_CKN
12H	PJ8	DSIHOST_CKP	13J	PJ9	DSIHOST_D0N
12J	PJ7	DSIHOST_D0P	-	-	-

1.1.5 LQFP64 package

The LQFP64 is available on the STM32F7x2xx devices.

1.2 Boot mode compatibility

The STM32F42xxx/F43xxx boot space is based on boot mode selection pins: BOOT0 and BOOT1 while the STM32F7 Series boot space is based on BOOT0 and boot address option bytes as described in *Table 6*.

For the STM32F74xxx/F75xxx devices, the boot base address supports any address in the range from 0x0000 0000 to 0x2004 FFFF while the STM32F76xxx/F77xxx devices extend the boot address to any address in the range from 0x0000 0000 to 0x2007 FFFF. The STM32F7x2xx/F7x3xx devices allow to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF.

Table 6. Boot mode selection comparison between the STM32F42xxx/F43xxx and STM32F7 Series devices

<table>
<tr><th colspan="4">STM32F7 Series</th></tr>
<tr><td colspan="2">Boot mode selection</td><td rowspan="2">Boot space</td></tr>
<tr><td>BOOT</td><td>Boot address Option Bytes</td></tr>
<tr><td>0</td><td>BOOT_ADD0 [15:0]</td><td>Boot address defined by user option byte BOOT_ADD0[15:0]
- ST programmed value: Flash on ITCM at 0x0020 0000</td></tr>
<tr><td>1</td><td>BOOT_ADD1 [15:0]</td><td>Boot address defined by user option byte BOOT_ADD1[15:0]
- ST programmed value: system bootloader at 0x0010 0000</td></tr>
<tr><th colspan="4">STM32F42xxx/F43xxx</th></tr>
<tr><td colspan="2">Boot mode selection Pins</td><td rowspan="2">Boot Mode</td><td rowspan="2">Aliasing</td></tr>
<tr><td>BOOT1</td><td>BOOT0</td></tr>
<tr><td>x</td><td>0</td><td>Main Flash memory</td><td>Main Flash memory is selected as the boot space at 0x0800 0000</td></tr>
<tr><td>0</td><td>1</td><td>System memory</td><td>System memory is selected as the boot space at 0x1FFF 0000</td></tr>
</table>

1.3 System bootloader

The system bootloader is located in the system memory, programmed by ST during the production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 7 shows the supported communication peripherals by the system bootloader.

Table 7. STM32F42xxx/F43xxx and STM32F7 Series bootloader communication peripherals

System bootloader peripherals	STM32F42xxx/F43xxx I/O pin	STM32F7 Series I/O pin
DFU	USB OTG FS (PA11 / PA12) in device mode	
USART1	PA9 / PA10	
USART3	PB10 / PB11 and PC10 / PC11	
CAN2 CAN1 in STM32F72xxx/F73xxx	PB5 / PB13 PB8/PB9	
I2C1	NA	PB6 / PB9
I2C2	NA	PF0 / PF1
I2C3	NA	PA8 / PC9
SPI1	NA	PA4 / PA5 / PA6 / PA7
SPI2	NA	PI0 / PI1 /PI2/ PI3
SPI4	NA	PE11 / PE12 / PE13 / PE14

By default, in the STM32F7 Series devices, when the boot from system bootloader is selected, the code is executed from the ITCM interface. It could be reprogrammed by option byte executed from the AXIM interface. For more details on system bootloader refer to AN2606.

2 Peripheral migration

2.1 STM32 product cross-compatibility

The STM32 series embed a set of peripherals which can be classed in three categories:

- The first category is for the peripherals which are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals which are shared by all STM32 products but have only minor differences (in general to support new features), so the migration from one product to another is very easy and does not need any significant new development effort.
- The third category is for peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, the migration will require a new development at application level.
- The SW compatibility mentioned in the *Table 8* only refers to the register description for "low level" drivers.

The Cube Hardware Abstraction Layer (HAL) is compatible between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 8 shows the STM32 peripheral compatibility between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 8. STM32 peripheral compatibility analysis between the STM32F42xxx/F43xxx and STM32F7 Series devices

Peripherals		STM32F42xxx /F43xxx	STM32F74xxx /F75xxx	STM32F76xxx /F77xxx	STM32F72xxx /F73xxx	Compatibility	
-		-		-	-	SW	Comments
Flash memory in Kbyte		2048	1024	2048	512	-	-
SRAM (Kbyte)	System	256 (115+16+64+ 64)	320 (240+16+64)	512 (386+16+128)	256 (176+16+64)		
	Instruction	NA	16	16	16		
	Backup	4	4	4	4		
Timers	GP	10	10	10	10	Yes	-
	Advanced control	2	2		2	Yes	-
	Basic	2	2		2	Yes	-
	Low-power	NA	1		1	NA	-

Table 8. STM32 peripheral compatibility analysis between the STM32F42xxx/F43xxx and STM32F7 Series devices (continued)

Peripherals		STM32F42xxx /F43xxx	STM32F74xxx /F75xxx	STM32F76xxx /F77xxx	STM32F72xxx /F73xxx	Compatibility	
Communication interfaces	Quad-SPI	No	Yes			NA	-
	SPI / I2S	6/2 (full duplex)	4/3 (simplex) 6/3 (simplex)(1)		3/3 (simplex) 4/3 (simplex) 5/3 (simplex)(2)	No/ Yes	I2S compatible.
	I2C	3	4		3	No	Programmable clock source for STM32F7 Series
	USART/ UART	4/4	4/4		4/4	No	Additional features on STM32F7 Series
	USB OTG FS	Yes	Yes		Yes	No	Dedicated VDDUSB More endpoints on STM32F7 Series
	USB OTG HS	Yes	Yes		Yes	No	More endpoints and host channels with an embedded HS PHY in the STM32F7x3 line
	CAN	2	2	3	1	Yes	-
	SAI	1	2			Yes	-
	SDIO/ SDMMC1	Yes	Yes	2x	2x	Yes	New clock source for SDMMC1 on STM32F7 Series with dedicated supply for SDM-MC2
	SPDIFRX	No	4 inputs		NA	NA	-
RNG		Yes	Yes		Yes	Yes	-
FMC memory con-troller		Yes	Yes		Yes	Yes	-
Ethernet		Yes	Yes		NA	Yes	-
MDIOS		No	No	Yes	NA	NA	-
HDMI-CEC		No	Yes		NA	NA	-
DCMI		Yes	Yes		NA	Yes	-
WWDG		Yes	Yes		Yes	Yes	-
IWDG		Yes	Yes		Yes	Yes	-
CRC		Yes	Yes		Yes	Yes	Additional features on STM32F7 Series
LCD-TFT		No | Yes(3)	Yes		NA	Yes	-

Table 8. STM32 peripheral compatibility analysis between the STM32F42xxx/F43xxx and STM32F7 Series devices (continued)

Peripherals		STM32F42xxx /F43xxx	STM32F74xxx /F75xxx	STM32F76xxx /F77xxx	STM32F72xxx /F73xxx	Compatibility	
DSI-HOST		No	No	Yes	NA	NA	New feature on STM32F7x9xx/ Fx8xx
JPEG		No	No	Yes	NA	NA	New feature on STM32F76xxx/ F77xxx
DMA		DMA1-DMA2 (8 stream each)				Yes	-
Chrom-ART-Acc (DMA2D)		Yes	Yes		NA	Yes	-
Crypto		Yes	Yes		Yes (AES256)	Yes	-
Hash		Yes	Yes		NA	Yes	-
GPIO		Up to 168	Up to 168		140 in STM32F7x2xx 138 in STM32F7x3xx	Yes	-
DFSDM1		No	No	4 filters	NA	NA	New feature on STM32F76xxx/ F77xxx
ADC	12 bits	3	3		3	Yes	ADC Timer Trigger not compatible
	Number of channels	16|24	16|24		16|24		
DAC	12 bits	Yes	Yes		Yes	Yes	-
	Number of channels	2	2		2		
EXTI		Yes	Yes		Yes	Yes	New EXTI line for LPTIM1
RCC		Yes	Yes		Yes	Yes	New LSE drive modes.
RTC		Yes	Yes		Yes	Yes	Additional features on STM32F7 Series
PWR		Yes	Yes		Yes	Yes	New wakeup pins with configurable polarity on STM32F7 Series
SYSCFG		Yes	Yes		Yes	Yes	-

1. SPI / I2S: 4/3 for 100 pin package and 6/3 for other packages.
2. SPI / I2S: 3/3 for 64 pin package, 4/3 for 100 pin package and 5/3 for other packages.
3. LCD - TFT:
   - No: not available for the STM32F437xx devices.
   - Yes: available for the STM32F439xx devices.

2.2 Memory mapping

Table 9 presents the peripheral address mapping differences between the STM32F42xxx/F43xx and STM32F7 Series devices.

Table 9. IP bus mapping differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

Peripheral	Bus	STM32F42xxx /F43xxx	STM32F74xxx /F75xxx	STM32F76xxx /F77xxx	STM32F72xxx /F73xxx
		Base address	Base address		Base address
Quad-SPI control register	AHB3	NA	0xA000 1000 - 0xA0001FFF		
SAI2	APB2	NA	0x4001 5C00 - 0x4001 5FFF		
HDMI-CEC	APB1	NA	0x4000 6C00 - 0x4000 6FFF		NA
I2C4		NA	0x4000 6000 - 0x4000 63FF		NA
I2S3ext		0x4000 4000 - 0x4000 43FF	NA		
SPDIFRX		NA	0x4000 4000 - 0x4000 43FF		NA
I2S2ext		0x4000 3400 - 0x4000 37FF	NA		
LPTIM1		NA	0x4000 2400 - 0x4000 27FF		
USB OTG PHY HS controller	APB2	NA	NA	NA	0x4001 7C00 - 0x4001 7FFF(1)
SDMMC2	APB2	NA	NA	0x4001 1C00 - 0x4001 1FFF	
DSI-HOST	APB2	NA	NA	0x4001 6C00 - 0x4001 73FF	NA
JPEG	AHB2	NA	NA	0x5005 1000 - 0x5005 1FFF	NA
CAN3	APB1	NA	NA	0x4000 3400 - 0x4000 37FF	NA
DFSDM1	APB2	NA	NA	0x4001 7400 - 0x4001 77FF	NA
MDIOS	APB2	NA	NA	0x4001 7800 - 0x4001 7BFF	NA

1. Only for the STM32F7x3xx devices.

2.3 Flash memory

Table 10 presents the differences between the Flash memory interface of the STM32F42xxx/F43xxx and STM32F7 Series devices.

The STM32F74xxx/F75xxx devices instantiate a different Flash module both in terms of architecture and interface. For more information on the programming, erasing and protection of the STM32F74xxx/F75xxx Flash memory, refer to the STM32F74xxx and STM32F75xxx reference manual (RM0385).

For more information on programming, erasing and protection of the STM32F76xxx/F77xxx Flash memory, refer to the STM32F76xxx and STM32F77xxx reference manual (RM0410).

For more information on programming, erasing and protection of the STM32F72xxx/F73xxx Flash memory, refer to the STM32F72xxx and STM32F73xxx reference manual (RM0431).

Table 10. Flash memory differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

Flash	STM32F42xxx /F43xxx	STM32F74xxx /F75xxx	STM32F76xxx /F77xxx	STM32F72xxx /F73xxx
Main/program memory	0x0800 0000 – 0x081F FFFF	0x0800 0000 - 0x080F FFFF (on AXIM interface)	0x0800 0000 - 0x080F FFFF (on AXIM interface)	0x0800 0000 - 0x0807 FFFF
	– Up to 2 Mbytes – Split in 2 banks – 4 sectors of 16 Kbytes – 1 sector of 64 Kbytes – 6 sectors of 128 Kbytes	– Up to 1 Mbyte – Split in 1 bank – 4 sectors of 32 Kbytes – 1 sector of 128 Kbytes – 3 sectors of 256 Kbytes	– Up to 2 Mbytes – configurable in 1 (or 2) bank (s) In single bank: – 4 sectors of 32 Kbytes – 1 sector of 128 Kbytes – 7 sectors of 256 Kbytes In dual bank: – Each bank is composed of: – 4 sectors of 16 Kbytes – 1 sector of 64 Kbytes – 7 sectors of 128 Kbytes	– Up to 512 Kbytes – Split in 1 bank – 4 sectors of 16 Kbytes – 1 sector of 64 Kbytes – 3 sectors of 128 Kbytes
Features	– 128 bit wide data read – Read while Write (RWW)	– 256 bit wide data read	– 256 bit wide data read in single Bank mode – 128 bit wide data read in dual Bank mode	– 128 bit wide data read
Wait State	Up to 8 (depending on the supply voltage and frequency)	Up to 9 (depending on the supply voltage and frequency)		
One time programmable (OTP)	512 OTP bytes	1024 OTP bytes		528 OTP bytes
Flash interface register	0x4002 3C00 - 0x4002 3FFF			

Table 10. Flash memory differences between the STM32F42xxx/F43xxx and STM32F7 Series devices (continued)

Flash		STM32F42xxx /F43xxx	STM32F74xxx /F75xxx	STM32F76xxx /F77xxx	STM32F72xxx /F73xxx
Option bytes	Base address	0x1FFF C000 - 0x1FFF C00F 0x1FFE C000 - 0x1FFE C00F	0x1FFF 0000 - 0x1FFF 001F (on AXIM interface)		
	FLASH_ OPTCR register	– Bit 31 SPRMOD – Bit 30 DB1M – Bits 29:28 Reserved – Bits 27:16 nWRP[11:0] – Bits 15:8 RDP – Bits 7:5 USER - Bit 7: nRST_STDBY - Bit 6: nRST_STOP - Bit 5: WDG_SW – Bit 4 BFB2 – Bits 3:2 BOR_LEV – Bit 1 OPTSTRT – Bit 0 OPTLOCK	– Bit 31 IWDG_STOP – Bit 30 IWDG_STDBY – Bits 29:24 Reserved – Bits 23:16 nWRP[7:0] – Bits 15:8 RDP[7:0] – Bits 7:4 USER - Bit 7: nRST_STDBY - Bit 6: nRST_STOP - Bit 5: IWDG_SW – Bit 4: WWDG_SW – Bits 3:2 BOR_LEV[1:0] – Bit 1 OPTSTRT – Bit 0 OPTLOCK	– Bit 31 IWDG_STOP – Bit 30 IWDG_STDBY – Bit 29 nDBANK – Bit 28 nDBOOT – Bits 27:16 nWRP[11:0] – Bits 15:8 RDP[7:0] – Bits 7:4 USER - Bit 7: nRST_STDBY - Bit 6: nRST_STOP - Bit 5: IWDG_SW – Bit 4: WWDG_SW – Bits 3:2 BOR_LEV[1:0] – Bit 1 OPTSTRT – Bit 0 OPTLOCK	– Bit 31 IWDG_STOP – Bit 30 IWDG_STDBY – Bits 29:24 Reserved – Bits 23:16 nWRP[7:0] – Bits 15:8 RDP[7:0] – Bits 7:4 USER - Bit 7: nRST_STDBY - Bit 6: nRST_STOP - Bit 5: IWDG_SW – Bit 4: WWDG_SW – Bits 3:2 BOR_LEV[1:0] – Bit 1 OPTSTRT – Bit 0 OPTLOCK
Memory protection		– Read protection (RDP) – Write protections – Proprietary code readout protection (PCROP)	– Read protection (RDP) – Write protections		– Read protection (RDP) – Write protections – Proprietary code readout protection (PCROP)

2.4 Embedded Flash memory

The main memory and information block organization are shown in *Table 11*.

Table 11. Flash module 1 Mbyte single bank organization (STM32F7 Series)

Block	Name	Bloc base addresses on AXIM interface		Block base addresses on ITCM interface		Sector size	
		STM32 F74xxx /F75xxx /F76xxx /F77xxx	STM32 F72xxx /F73xxx	STM32 F74xxx /F75xxx /F76xxx /F77xxx	STM32 F72xxx /F73xxx	STM32 F74xxx/ F75xxx /F76xxx /F77xxx	STM32 F72xxx /F73xxx
Main memory block	Sector 0	0x0800 0000 - 0x0800 7FFF	0x0800 0000 - 0x0800 3FFF	0x0020 0000 - 0x0020 7FFF	0x0020 0000 - 0x0020 3FFF	32 Kbytes	16 Kbytes
	Sector 1	0x0800 8000 - 0x0800 FFFF	0x0800 4000 - 0x0800 7FFF	0x0020 8000 - 0x0020 FFFF	0x0020 4000 - 0x0020 7FFF	32 Kbytes	16 Kbytes
	Sector 2	0x0801 0000 - 0x0801 7FFF	0x0800 8000 - 0x0800 BFFF	0x0021 0000 - 0x0021 7FFF	0x0020 8000 - 0x0020 BFFF	32 Kbytes	16 Kbytes
	Sector 3	0x0801 8000 - 0x0801 FFFF	0x0800 C000 - 0x0800 FFFF	0x0021 8000 - 0x0021 FFFF	0x0020 C000 - 0x0020 FFFF	32 Kbytes	16 Kbytes
	Sector 4	0x0802 0000 - 0x0803 FFFF	0x0801 0000 - 0x0801 FFFF	0x0022 0000 - 0x0023 FFFF	0x0021 0000 - 0x0021 FFFF	128 Kbytes	64 Kbytes
	Sector 5	0x0804 0000 - 0x0807 FFFF	0x0802 0000 - 0x0803 FFFF	0x0024 0000 - 0x0027 FFFF	0x0022 0000 - 0x0023 FFFF	256 Kbytes	128 Kbytes
	Sector 6	0x0808 0000 - 0x080B FFFF	0x0804 0000 - 0x0805 FFFF	0x0028 0000- 0x002B FFFF	0x0024 0000 - 0x0025 FFFF	256 Kbytes	128 Kbytes
	Sector 7	0x080C 0000 - 0x080F FFFF	0x0806 0000 - 0x0807 FFFF	0x002C 0000 - 0x02F FFFF	0x0026 0000 - 0x0027 FFFF	256 Kbytes	128 Kbytes
Information block	System memory	0x1FF0 0000 - 0x1FF0 EDBF	0x1FF0 0000 - 0x1FF0 76D7	0x0010 0000- 0x0010 EDBF	0x0010 0000- 0x0010 76D7	60 Kbytes	30 Kbytes
	OTP	0x1FF0 F000 - 0x1FF0 F41F	0x1FF0 7800- 0x1FF0 7A0F	0x0010 F000 - 0x0010 F41F	0x0010 7800 - 0x0010 7A0F	1024 bytes	528 bytes
	Option bytes	0x1FFF 0000 - 0x1FFF 001F		-		32 bytes	

2.5 Flexible memory controller (FMC)

Table 12 presents the FMC differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 12. FMC differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

FMC		STM32F42xxx/F43xxx	STM32F7 Series
External memory interfaces		– SRAM – NOR/NAND memories – PSRAM – Two banks of NAND Flash memory with ECC hardware – 16-bit PC Card compatible devices	– SRAM – NOR/NAND memories – PSRAM – NAND Flash memory with ECC hardware
Data bus width		8-,16- or 32-bit	
FMC Bank memory mapping	Bank1 4×64 Mbytes	NOR/PSRAM/SRAM	NOR/PSRAM/SRAM
	Bank2 4×64 Mbytes	NAND Flash memory	Reserved
	Bank3 4×64 Mbytes		NAND Flash memory
	Bank4 4×64 Mbytes	PC Card	Reserved
	SDRAM bank1 4×64 Mbytes	SDRAM	SDRAM
	SDRAM bank2 4×64 Mbytes		
Memory mapping swap: (SYSCFG_MEMRMP) Bits 11:10 SWP_FMC[1:0] = 01b		NOR/PSRAM/SRAM 256 Mbytes	SDRAM bank1 256 Mbytes
		NAND bank1 256 Mbytes	SDRAM bank2 256 Mbytes
		SDRAM bank1 256 Mbytes	NAND bank3 256 Mbytes
		SDRAM bank2 256 Mbytes	Reserved
		Reserved	Reserved
		NAND bank2 256 Mbytes	NOR/PSRAM/SRAM 256 Mbytes
		PC card 256 Mbytes	Reserved

2.6 Interrupt vectors

Table 13 presents the interrupt vector differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 13. Interrupt vector differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

Position	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx	STM32F76xxx/F77xxx	STM32F72xxx/F73xxx
91	NA	SAI2		
92	NA	Quad-SPI		
93	NA	LPTIM1		
94	NA	HDMI-CEC		NA
95	NA	I2C4_EV		NA
96	NA	I2C4_ER		NA
97	NA	SPDIFRX		NA
98	NA	NA	DSIHOST	NA
99	NA	NA	DFSDM1_FLT0	NA
100	NA	NA	DFSDM1_FLT1	NA
101	NA	NA	DFSDM1_FLT2	NA
102	NA	NA	DFSDM1_FLT3	NA
103	NA	NA	SDMMC2	SDMMC2
104	NA	NA	CAN3_TX	NA
105	NA	NA	CAN3_RX0	NA
106	NA	NA	CAN3_RX1	NA
107	NA	NA	CAN3_SCE	NA
108	NA	NA	JPEG	NA
109	NA	NA	MDIOS	NA

2.7 External interrupt lines (EXTI)

Table 14 presents the EXTI line differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 14. EXTI line differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

EXTI line	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx	STM32F76xxx/F77xxx	STM32F72xxx/73xxx
0 to 15	16 external interrupt lines			
16	PVD output			
17	RTC alarm event			
18	USB OTG FS wakeup event			
19	Ethernet wakeup event			NA
20	USB OTG HS (configured in FS) wakeup event			
21	RTC tamper and TimeStamp events			
22	RTC wakeup event			
23	NA	LPTIM1 asynchronous event		
24	NA	NA	MDIO slave asynchronous event	NA

2.8 RCC

Table 15 presents the main differences related to the RCC (Reset and Clock Controller) between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 15. RCC differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

Peripherals	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx/ F76xxx/F77xxx/F7x2xx	STM32F7x3xx
	Clock sources		
USB OTG FS	– PLL48MHz derived from main PLL VCO (PLLQ Clock)	– PLL48MHz derived from main PLL VCO (PLLQ Clock) – PLLSAI VCO (PLLSAI clock)	
RNG			
SDIO/SDMMC1	– PLL48CLK	– PLL48CLK – SYSCLK	
U(S)ARTs	– APB1 or APB2 clock (PCLK1 or PCLK2)	– System clock (SYSCLK) – HSI clock – LSE clock – APB1 or APB2 clock (PCLK1 or PCLK2)	
I2Cs	– APB1 clock (PCLK1)	– System clock (SYSCLK) – HSI clock – APB1 or APB2 clock (PCLK1 or PCLK2)	
I2S	– PLLI2S – External clock mapped on I2S_CKIN pin		
SAI1	– PLLI2S_Q – PLLSAI_Q – External clock mapped on the I2S_CKIN pin.		
SAI2	NA	– PLLI2S_Q – PLLSAI_Q – External clock mapped on the I2S_CKIN pin.	
LTDC	– PLLSAI_R		NA
LPTIM1	NA	– LSI clock – LSE clock – HSI clock – APB1 clock (PCLK1)	
USB OTG HS	– 24 to 60 MHz to external PHY		The STM32F7x3xx devices embed an USB OTG PHY HS. The PHY HS has two PLLs: PLL1 and PLL2. The PLL1 allows to output 60 MHz used as an input for PLL2 which itself allows to generate the 480 Mbps in the USB OTG High Speed mode. The PLL1 has as input HSE clock.
ETHERNET MAC	– 25 to 50 MHz external PHY		NA

Table 15. RCC differences between the STM32F42xxx/F43xxx and STM32F7 Series devices (continued)

Peripherals	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx/ F76xxx/F77xxx/F7x2xx	STM32F7x3xx
	Clock sources		
SPDIFRX	NA	– PLLI2SP VCO	NA
HDMI-CEC	NA	– LSE clock – HSI clock divided by 488	NA
RTC	– LSE clock – LSI clock – HSE clock divided by 32		
IWDG	LSI		
LSE	NA	Configurable LSE drive in RCC_BDCR register: LSEDRV[1:0]: – 00: Low drive – 10: Medium low drive – 01: Medium high drive – 11: High drive	
RCC dedicated clock configuration register	– RCC_DCKCFGR	– RCC_DKCFGR1 – RCC_DKCFGR2	

2.8.1 Maximum frequency according to power scale parameter

Table 16 shows the comparison of maximum frequency that the MCU can reach between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 16. Maximum frequency comparison between the STM32F42xxx/F43xxx and STM32F7 Series devices

Symbol	Parameter	Conditions		F4 max Freq	F7 max Freq	Unit
f_{HCLK}	Internal AHB clock frequency	Power scale 3 (Over-drive OFF)		120	144	MHz
		Power scale 2	Over-drive OFF	144	168	
			Over-drive ON	168	180	
		Power scale 1	Over-drive OFF	168	180	
			Over-drive ON	180	216	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		42	45	
		Over-drive ON		45	54	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		84	90	
		Over-drive ON		90	108	

2.9 PWR

Table 17 presents the PWR controller differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 17. PWR differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

PWR	STM32F42xxx/F43xxx	STM32F7 Series
Power supplies	NA	– Independent USB transceivers supply: VDDUSB: range is from 3.0 V to 3 6 V and is completely independent from VDD or VDDA – VDDSDMMC2 supply: range is from 1.7 V to 3.6 V and it can be independent from VDD (only on STM32F76xxx/F77xxx and STM32F72xxx/F73xxx devices).
Standby mode wakeup sources	– WKUP pin PA0 on rising edge – RTC event (RTC ALARM, Tamper event,Time stamp event) – IWDG reset – External reset in NRST pin	– WKUP pin with configurable polarity on rising or falling edge: – PA0 – PA2 – PC1 – PC13 – PI8 – PI11 – RTC event (RTC ALARM, tamper event, time stamp event) – IWDG reset – External reset in NRST pin
Power control registers	PWR_CR PWR_CSR	PWR_CR1 PWR_CSR1
	NA	PWR_CR2 PWR_CSR2 Comment : – PWR_CR2: Used to configure the wakeup pin polarity, or to clear the wakeup pins flags. – PWR_CSR2: Used either to enable the wakeup pins or used to detect an event on the wakeup pin

2.10 RTC

Table 18 shows the RTC comparison between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 18. RTC comparison between the STM32F42xxx/F43xxx and STM32F7 Series devices

RTC	STM32F42xxx/F43xxx	STM32F7 Series
Calendar in BCD	Yes	
Calendar sub seconds access	Yes Resolution down to RTCCLK	
Calendar synchronization on-the-fly	Yes	
Alarm on calendar	2 w/ sub second	
Calendar calibration	Calibration window: 8s/16s/32s Calibration step: 3.81ppm/1.91ppm/0.95 ppm Range [-480ppm +480ppm]	
Synchronization on mains	Yes	
Periodic wakeup	Yes	
Timestamp	Yes Sec, Min, Hour, Date, Sub seconds	
Timestamp on VBAT switch	No	Yes
Tamper	2 pins/ 2 events	3 pins/ 3 events
	Edge or level detection with configurable filtering	
External interrupt and trigger with filtering	No	Yes
32-bit backup registers	20	32
RTC in VBAT	Yes	

2.11 U(S)ART

The U(S)ART is not SW compatible with the STM32F42xxx/F43xxx devices and includes new additional features detailed in *Table 19*.

Table 19. U(S)ART differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

U(S)ART	STM32F42xxx/F43xxx	STM32F7 Series
UART/USART	4/4	
Baud rate	– Up to 4x11.25 Mbit/s	– Up to 27 Mbit/s – (clock frequency is 100 MHz and oversampling is by 8)
Clock	– Single clock domain	– Dual clock domain: Convenient baud rate programming independent from the PCLK reprogramming
Data	– Word length: Programmable (8 or 9 bits)	– Word length: Programmable (7, 8 or 9 bits) – Programmable data order with MSB-first or LSB-first shifting
interrupt	– 10 interrupt sources with flags	– 14 interrupt sources with flags
Features	– LIN mode – SPI Master – IrDA SIR ENDEC block – Hardware flow control (CTS/RTS) – Continuous communication using DMA – Multiprocessor communication – Single-wire half-duplex communication	
	Smartcard mode T = 0 and T= 1 has to be implemented by software. Number of stop bits: 0.5, 1, 1.5, 2	Support the T=0 and T=1 asynchronous protocols. Number of stop bits: 0.5, 1, 1.5, 2 smartcard operation.
	NA	– Support for ModBus communication - Timeout feature - CR/LF character recognition – Receiver timeout interrupt – Auto baud rate detection – Driver Enable – Swappable Tx/Rx pin configuration
U(S)ART registers	– Software not compatible	

2.12 I2C

The STM32F42xxx/F43xxx and STM32F7 Series devices share the same features on the I2C, but the software and register configuration are not compatible.

Table 20 presents the I2C differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 20. I2C differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

I2C	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx/ F76xxx/F77xxx	STM32F72xxx/F73xxx
Instances	– x3 (I2C1, I2C2, I2C3)	– x4 (I2C1, I2C2, I2C3, I2C4)	– x3 (I2C1, I2C2, I2C3)
Features	– 7-bit and 10-bit addressing mode – SMBus – Standard mode (up to 100 kbit/s) – Fast-mode (up to 400 kbit/s)		
	-	– Fast-mode plus (up to 1 Mbit/s)(1)	
	– Single clock source	– Programmable clock source	
I2C registers	– Software not compatible.		

1. On the STM32F77xxx/F76xxx/F72xxx/F73xxx devices, the I2C I/Os support the 20mA drive needed in Fast-mode Plus.

2.13 SPI

The STM32F42xxx/F43xxx and STM32F7 Series implement different features on the SPI.

Table 21 presents the SPI differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 21. SPI differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

SPI	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx/ F76xxx/F77xxx	STM32F72xxx/F73xxx
Instances	x6	x4 | x6	x3 | x5
Features	SPI + I2S		
Data size	Fixed, configurable to 8 or 16 bits	Programmable from 4 to 16-bit	
Data buffer	Tx & Rx 16-bit buffers (single data frame)	Two 32-bit embedded Rx and Tx FIFOs (up to 4 data frames)	
Data packing	No (16-bit access only)	Yes	
Mode	SPI TI mode SPI Motorola mode	SPI TI SPI Motorola mode NSSP mode	
Speed	Up to 45 Mbit/s	Up to 54 Mbit/s	
SPI registers	Software not compatible		

2.14 CRC

The STM32F7 Series devices implements a similar CRC (Cyclic redundancy check) calculation unit as the STM32F42xxx/F43xxx devices.

Table 22 presents the CRC differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 22. CRC differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

CRC	STM32F42xxx/F43xxx	STM32F7 Series
Features	– Single input/output 32-bit data register – CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size – General-purpose 8-bit register (can be used for temporary storage)	
	– Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7 – Handles 32-bit data size	– Fully programmable polynomial with programmable size (7, 8, 16, 32bits) – Handles 8-,16-, 32-bit data size – Programmable CRC initial value – Input buffer to avoid bus stall during calculation – Reversibility option on I/O data
CRC registers	– Software compatible. – STM32F7 Series includes new features.	

2.15 USB OTG

Table 23 presents the USB OTG differences between the STM32F42xxx/F43xxx and STM32F7 Series devices.

Table 23. USB OTG differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

USB	STM32F42xxx/F43xxx	STM32F7 Series
Features	– Universal Serial Bus revision 2.0 – Full support for the USB On-The-Go (USB OTG).	
	FS mode: – 1 bidirectional control endpoint – 3 IN endpoints (bulk, interrupt, isochronous) – 3 OUT endpoints (bulk, interrupt, isochronous – HS mode: – 6 bidirectional endpoints (including EP0) – 12 host mode channels	FS mode: – 1 bidirectional control endpoint – 5 IN endpoints (bulk, interrupt, isochronous) – 5 OUT endpoints (bulk, interrupt, isochronous) HS mode:(1) – 9 bidirectional endpoints (including EP0) – 16 host channels with periodic OUT support
	– USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line.	
	NA	– Independent VDDUSB power supply allowing lower VDDCORE while using USB.
Buffer memory	FS mode: – 1.25 Kbytes data FIFOs – Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO. HS mode: – 4 Kbytes total RAM	FS mode: – 1.25 Kbytes data FIFOs – Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO. HS mode: – 4 Kbytes total RAM
Low-power modes	FS mode: – USB suspend and resume HS mode: – No LPM supported	FS mode: – USB suspend and resume – Link power management (LPM) support HS mode: – Yes LPM supported
Configuration	– SW not compatible	

1. In the STM32F42xxx/43xxx and STM32F74xxx/F75xxx/F76xxx/F77xxx/F7x2xx devices, the HS mode is supported via ULPI interface.

   In the STM32F7x3xx devices, the HS mode is supported based on an embedded PHY high speed.

2.16 ADC

The STM32F7 Series devices embed the same ADC peripherals with the same features except for external triggers in regular and injected channels.

Table 24 and *Table 25* present the differences of external trigger for regular channels and injected channels between the STM32F42xxx/F43xxx and STM32F7 Series devices.

2.16.1 External trigger for regular channels

Table 24. External trigger for regular channel differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

Type	EXTSEL[3:0]	Source	
		STM32F42xxx/F43xxx	STM32F7 Series
Internal signal from on-chip timers	0000	TIM1_CH1 event	TIM1_CC1 event
	0001	TIM1_CH2 event	TIM1_CC2 event
	0010	TIM1_CH3 event	TIM1_CC3 event
	0011	TIM2_CH2 event	TIM2_CC2 event
	0100	TIM2_CH3 event	TIM5_TRGO event
	0101	TIM2_CH4 event	TIM4_CC4 event
	0110	TIM2_TRGO event	TIM3_CC4
	0111	TIM3_CH1 event	TIM8_TRGO event
	1000	TIM3_TRGO event	TIM8_TRGO(2) event
	1001	TIM4_CH4 event	TIM1_TRGO event
	1010	TIM5_CH1 event	TIM1_TRGO(2) event
	1011	TIM5_CH2 event	TIM2_TRGO event
	1100	TIM5_CH3 event	TIM4_TRGO event
	1101	TIM8_CH1 event	TIM6_TRGO event
	1110	TIM8_TRGO event	NA
External pin	1111	EXTI line11	

2.16.2 External trigger for injected channels

Table 25. External trigger for injected channel differences between the STM32F42xxx/F43xxx and STM32F7 Series devices

Type	EXTSEL[3:0]	Source	
		STM32F42xxx/F43xxx	STM32F7 Series
Internal signal from on-chip timers	0000	TIM1_CH4 event	TIM1_TRGO event
	0001	TIM1_TRGO event	TIM1_CC4 event
	0010	TIM2_CH1 event	TIM2_TRGO event
	0011	TIM2_TRGO event	TIM2_CC1 event
	0100	TIM3_CH2 event	TIM3_CC4 event
	0101	TIM3_CH4 event	TIM4_TRGO event
	0110	TIM4_CH1 event	NA
	0111	TIM4_CH2 event	TIM8_CC4 event
	1000	TIM4_CH3 event	TIM1_TRGO(2) event
	1001	TIM4_TRGO event	TIM8_TRGO event
	1010	TIM5_CH4 event	TIM8_TRGO(2) event
	1011	TIM5_TRGO event	TIM3_CC3 event
	1100	TIM8_CH2 event	TIM5_TRGO event
	1101	TIM8_CH3 event	TIM3_CC1 event
	1110	TIM8_CH4 event	TIM6_TRGO event
External pin	1111	EXTI line15	NA

3 Conclusion

This application note is a useful complement to the datasheets and reference manuals, which gives a simple guideline to migrate from an existing STM32F42xxx/F43xxx device to a STM32F7 Series device.

4 Revision history

Table 26. Document revision history

Date	Revision	Changes
31-Mar-2015	1	Initial release.
29-May-2015	2	Updated: – *Section 2.1: STM32 product cross-compatibility* with a new paragraph about software compatibility, – *Table 8: STM32 peripheral compatibility analysis between the STM32F42xxx/F43xxx and STM32F7 Series devices* for RNG, ADC, and DAC peripherals, – *Section 2.8.1: Maximum frequency according to power scale parameter* setting F7 max at 216 MHz, 108 MHz and 54 MHz in over-drive ON conditions, – *Section 2.11: U(S)ART* with baud rate up to 13.5 Mbit/s.
13-Feb-2017	3	Updated whole document to address the STM32F7 Series devices. Added: – *Section 1.1.2: LQFP208 package*. – *Section 1.1.3: LQFP176 package*. – *Section 1.1.4: TFBGA216 package*. Updated: – *Table 8: STM32 peripheral compatibility analysis between the STM32F42xxx/F43xxx and STM32F7 Series devices*. – *Table 9: IP bus mapping differences between the STM32F42xxx/F43xxx and STM32F7 Series devices*. – *Table 10: Flash memory differences between the STM32F42xxx/F43xxx and STM32F7 Series devices*. – *Table 13: Interrupt vector differences between the STM32F42xxx/F43xxx and STM32F7 Series devices*. – *Table 14: EXTI line differences between the STM32F42xxx/F43xxx and STM32F7 Series devices*.